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A Study of Nanowire Junctions and Their Impact on the Properties of Nanowire Networks
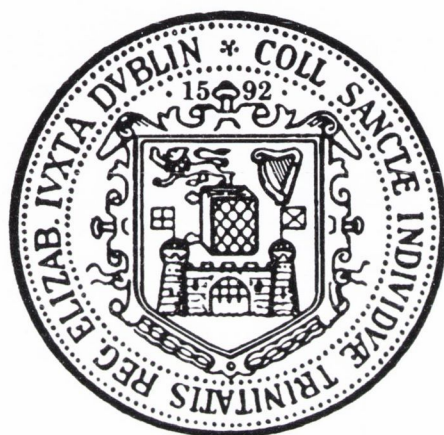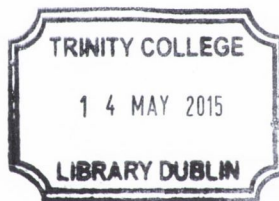
A thesis presented to the University of Dublin, Trinity College

for the degree of

Doctor of Philosophy in Chemistry

by

Allen T. Bellew

Under the supervision of Prof. John Boland

School of Chemistry & CRANN
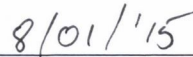
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2015

DECLARATION

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SUMMARY

Nanowire networks are of immense technological interest due to their properties of high transparency, high porosity, flexibility, ease of fabrication, and low cost. Despite the increasing attention these materials continue to receive, there remains a fundamental lack of understanding in the literature regarding the properties of the basic building block of nanowire networks – the nanowire junction. This is highlighted by several recent reports in the literature that attempt to extract the resistance of the junction from bulk measurements, producing inconsistent results. This thesis focuses on addressing this lack of understanding by examining individual junctions composed of both silver and nickel nanowires with passivating surface layers. Passivation layers are ubiquitous throughout nanoscience, and are generally seen as obstacles that must be overcome in order to realise functional devices or applications. Rather than seeing them as obstacles however, this thesis utilises these passivation layers as device components in and of themselves, and in doing so demonstrates the addition of new levels of functionality into otherwise simple, metallic systems.

The junction resistance of Ag nanowires was determined through a carefully designed measurement, accounting for both the contact resistance and the resistance contribution of the nanowire length. This was performed for both untreated Ag nanowires, and those that had been thermally annealed to remove the insulating polymer coating. Thermally treated nanowires demonstrated remarkably low junction resistances, less than $50\,\Omega$, while it was found that the untreated nanowires were insulating in the pristine state due to the presence of polymer at the junction interface. Through the application of a sufficiently large voltage (1–2 V), this layer was broken down to form a highly conductive connection. By driving current through this electroformed junction, low junction resistances ($< 60\,\Omega$) were obtained. The results of both thermally activated and electroformed junctions were combined to generate the first measured distribution of junction resistances for Ag nanowires. The junction resistance of Ni nanowires was also determined. A nanoscale passivating layer of NiO forms on the surface of Ni nanowires, creating a core-shell structure. As a well known resistive switching material, the reversible electrical breakdown of NiO is extremely well studied. This mechanism was employed to create an ohmic connection between the two metal cores of a Ni nanowire junction, and thereby allow the resistance to be measured. A distribution of junction resistances was obtained across several nanowire junctions, showing an average value of $718\,\Omega$.

The effect of nanoscale surface passivation layers on the behaviour of nanowire networks was studied by first examining the electrical activation of untreated Ag nanowire networks. Prior work established the dependence of activation voltage on the inter-electrode distance and nanowire density, and a model was developed to describe this behaviour based on the formation of cells of activated nanowires. Building upon this, a study was undertaken examining the behaviour of untreated Ag nanowire networks as a function of network size.

It was found that as a network was electrically stressed post-activation, the conductance of the network increased due to both a reduction of the junction resistance and the addition of parallel conducting pathways. This behaviour was collectively termed connectivity evolution. It was discovered that the degree to which a network may evolve its connectivity is dependent upon the network size, as smaller networks demonstrated almost complete connectivity, while for larger networks there remained non-activated parallel paths even with the application of high electric fields.

The electrical behaviour of Ni nanowire networks was also examined as a function of network size. It was found that small networks demonstrated the same resistive switching behaviour as single junctions, and it was concluded that this was due to the existence of a single junction acting as a bottle-neck point for the current. It was found that the probability of observing resistive switching behaviour fell off as the network size increased, eventually becoming zero. At these large network sizes, networks demonstrated the same connectivity evolution behaviour seen for Ag networks. This demonstrated the existence of two behavioural regimes defined by the network size: device-like, and material-like behaviour. Finally these results were combined to fabricate a programmable network, where both a resistive switching device and a metallic interconnect material were fabricated into the same network. These results from analysis of the current-voltage behaviour were complemented by the development of passive voltage contrast imaging techniques that allowed for the visualisation of conductive pathways through a network. Utilising both the scanning electron microscope and the helium ion microscope, two separate PVC techniques were developed for the visualisation of Ag and Ni networks respectively. Using these techniques, the theory of connectivity evolution through the addition of parallel pathways was validated.

Ultimately, this thesis demonstrates that in order to gain a full and complete understanding of the properties of networks, the junctions that make up that network must be fully characterised in isolation. In addition to this, it has been shown that the incorporation of non-linear elements such as resistive switches at the junctions introduces new levels of functionality such as programmability, and that this may be controlled through the network geometry defined by the interrogating electrodes. These results are fascinating from a phenomenological perspective, but may also prove valuable from a device perspective as technology moves towards flexible, multi-functional, and multi-sensory platforms.

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LIST OF ABBREVIATIONS

AFM	Atomic Force Microscope
AAO	Anodised Aluminium Oxide
BSE	Backscattered Electron
CAFM	Conductive Atomic Force Microscopy
CNT	Carbon Nanotube
CVU	Capacitance Voltage Unit
DUT	Device Under Test
ECM	Electrochemical Metallization Memory
EBL	Electron Beam Lithography
EDX	Energy Dispersive X-ray Spectroscopy
FEG	Field Emission Gun
FIB	Focused Ion Beam
HIM	Helium Ion Microscope
HRS	High Resistance State
ITRS	International Technology Roadmap for Semiconductors
LRS	Low Resistance State
MMA	Poly(methyl methacrylate – methacrylic acid)
MRAM	Magnetic Random Access Memory
PCM	Phase Change Memory
PMMA	Poly(methyl methacrylate)
PMU	Pulse Measure Unit

PVC   Passive Voltage Contrast

PVP   Polyvinylpyrrolidone

ReRAM   Redox Random Access Memory

RS   Resistive Switching

SE   Secondary Electron

SEM   Scanning Electron Microscope

SMU   Source Measure Unit

TCO   Transparent Conducting Oxide

TEM   Transmission Electron Microscope

TMO   Transition Metal Oxide

LIST OF PUBLICATIONS

[1] LYONS, P.E., DE, S., ELIAS, J., SCHAMEL, M., PHILIPPE, L., BELLEW, A.T., BOLAND, J.J., & COLEMAN, J.N., *The Journal of Physical Chemistry Letters* **2011**, *2*, 3058–3062.

[2] NIRMALRAJ, P.N., BELLEW, A.T., BELL, A.P., FAIRFIELD, J.A., MC-CARTHY, E.K., O'KELLY, C., PEREIRA, L.F.C, SOREL, S., MOROSAN, D., COLEMAN, J.N., FERREIRA, M.S., & BOLAND, J.J., *Nano Letters* **2012**, *12*, 5966–5971.

[3] BELLEW, A.T., BELL, A.P., MCCARTHY, E.K., FAIRFIELD, J.A., & BOLAND, J.J., *Nanoscale* **2014**, *6*, 9632–9639.

[4] MCCARTHY, E.K., BELLEW, A.T., SADER J.E., & BOLAND, J.J., *Nature Communications* **2014**, *5*.

[5] FAIRFIELD, J.A., RITTER, C., BELLEW, A.T., MCCARTHY, E.K., FER-REIRA, M.S., & BOLAND, J.J., *ACS Nano* **2014**, *8*, 9542–9549.

1

INTRODUCTION

Equipped with his five senses, man explores the universe around him and calls the adventure science.

– Edwin Hubble

For more than half a century, the ideas and advances brought about by nanoscience have helped dictate the shape of the world around us. In 1971, Intel released its first commercially available microprocessor chip, which contained a total of 2,300 transistors. Today, standard chips contain transistors numbering in the billions – an advancement made possible by the breakthroughs made in nanoscience. From solar cell technology, to faster, more powerful and more efficient electronics, to advanced sports equipment, nanoscience continues to be the driving force behind many of the technologies that govern our modern world. The great physicist Richard Feynman – considered by many to be the father of nanoscience – once eloquently described it as "there's plenty of room at the bottom",[1] describing the vast amounts of information that could be stored in a space no larger than the head of a pin, but also foretelling the enormous advancements that could be made if the nano-world was harnessed. Exploring the electrical behaviour of nanoscale objects, both collectively and in isolation, this thesis aims to contribute to this now vast field, and advance the collective knowledge a little further.

Nanoscience is an all-encompassing term, describing the study of all matter smaller than 100 nanometres (nm) in any dimension. One subset of this that continues to receive ever growing attention is the study of low-dimensional materials. These novel materials, many of which have only recently been discovered or fabricated for the first time, fall into three categories: zero-dimensional (0-D), one-dimensional (1-D), and two dimensional (2-D). 0-D materials include quantum dots and nanoparticles – materials that are "small" in all dimensions, and are thus pseudo 0-D, while 2-D describes the newest arrivals to the nano-scene, materials of macroscopic length in two dimensions, but of incredibly low dimension in the third. Examples of these include graphene[2] and its various inorganic counterparts[3]. The third category, 1-D, includes materials such as nanotubes and nanowires – materials of

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nanoscale size in two dimensions, but macroscale in the third, and it is on these materials that this thesis shall focus.

Upon their discovery in 1991,[4] carbon nanotubes (CNTs) were heralded as a wonder material due to their exciting properties of high strength and high electron mobility, and their pseudo 1-D nature meant the possibility of extremely high device integration densities. In the following two decades the fervour has died down considerably, due in part to the variation in conduction properties that are dependent upon the chirality of the nanotube, and the extremely difficult challenges associated with accurate placement of single nanoscale entities. 1-D materials still provide many opportunities for novel materials and devices however, though the focus of modern research has shifted largely to metallic and semiconducting nanowires, due to a greater diversity of properties and an ability to more accurately control these based on growth conditions. With a multitude of different fabrication techniques, from vapour-liquid-solid (VLS) growth[5] and sol-gel approaches,[6] to electrochemical deposition,[7] nanowires may be formed from a wide range of materials. This diversity has resulted in nanowires finding an equally wide range of applications, including field-effect transistors,[8,9] gas sensors,[10] and electromechanical switches.[11,12] Despite the many promising results that have emerged, commercial application of any of these technologies has yet to be realised, again reflecting the extreme difficulty associated with placement of nanoscale entities on a large, reproducible scale.

One technique to overcome the difficulties associated with individual nanowires but retain many of the promising characteristics of these materials is to form networks of interconnected nanowires. Although for the most part this precludes the use of nanowires in device applications,* the obvious advantage of such a material is that accurate placement of the nanowires is no longer a concern. Networks also average out the properties of individual nanowires, the variation of which can be significant, and therefore allow for less stringent fabrication processes, reducing cost. Perhaps one of the most noteworthy advantages of network materials is their intrinsic flexibility and optical transmittance at low nanowire loading,[13] enabling their use in advanced flexible electronics which are likely to dominate the market in the coming decade.[14] This thesis studies transparent networks of both silver and nickel nanowires, and in particular looks at the connectivity within these networks and how this may be manipulated through the use of active and passive nanowire coatings.

Passivation layers are ubiquitous throughout the field of nanoscience. In order to prevent aggregation of nanostructures, a surface layer must be used to passivate the surface – common examples of passivation layers include polymers, molecules such as citrate or thiols, or even naturally forming oxides. While crucial for the fabrication and stabilisation of nanostructures, these passivation layers must then be removed before a functional device or technology can be realised, and thus present a major barrier to the incorporation of nano-materials in new technologies. An alternative approach to the use of passivation layers is to see them as device components in and of themselves, rather than obstacles that must be overcome. This new paradigm will lead to greater levels of functionality within

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*This thesis demonstrates how devices may be fabricated from random networks.

not only single nanowire devices, but networks also, while at the same time also reducing processing steps, saving both time and money. The work presented in this thesis strives to demonstrate how passivation layers may introduce new levels of functionality to otherwise simple metallic materials.

This chapter begins with a discussion of nanowire networks, introducing the reader to the field and discussing the state-of-the-art. Resistive switching shall then be introduced, and an extensive literature review provided, as this is central to the mechanism for introducing added functionality through the use of passivation layers. Recent advances in both of these concepts shall also be discussed. These sections aim to give the reader a strong foundation in these fundamental concepts, from which the subsequent chapters will build to demonstrate how random nanowire networks may be designed to produce new material properties and ultimately provide a method to fabricate multi-functional, programmable networks.

1.1 NANOWIRE NETWORKS

The nanowire network was first introduced by Huang et al. in 2001, where they fabricated well aligned, perpendicular arrays of semiconducting nanowires using a directed fluidic approach.[15] This work proved to be the beginnings of a field that would grow to considerable size; Figure 1.1 illustrates this by showing the year-on-year increase in both publications and citations for articles including the term "nanowire network", since 2001. Although the original paper by Huang et al. described only modest networks consisting of very few nanowires, the term has been broadened considerably since then and in general describes a random arrangement of nanowires on a surface, such that a continuous path may be drawn from one side to the other, i.e. the surface density is beyond the threshold required for percolation. This sharp rise in research into these materials is a direct reflection of the intrinsic material properties that they possess, including optical transparency, flexibility, high porosity, ease of fabrication, and low cost. As a result of these remarkable properties, networks have been incorporated into a wide range of applications, including artificial skin,[16,17] and gas sensing.[18,19] The most successful of these to date however, has been the development of transparent conductors from nanowire networks. The following section is devoted to describing this work.

1.1.1 NANOWIRE NETWORKS FOR TRANSPARENT CONDUCTOR APPLICATIONS

Transparent conducting thin films make possible many of the technologies we now take for granted. Liquid-crystal displays (LCDs), organic light emitting diodes (OLEDs), touch screens, solar cells, and e-readers all require materials that have both high optical transparency and high electrical conductivity. For nearly four decades, transparent conducting oxides (TCOs) such as tin-doped indium oxide (ITO) and fluorine-doped tin oxide (FTO) have dominated this market.[21] However, as the market begins to shift towards flexible
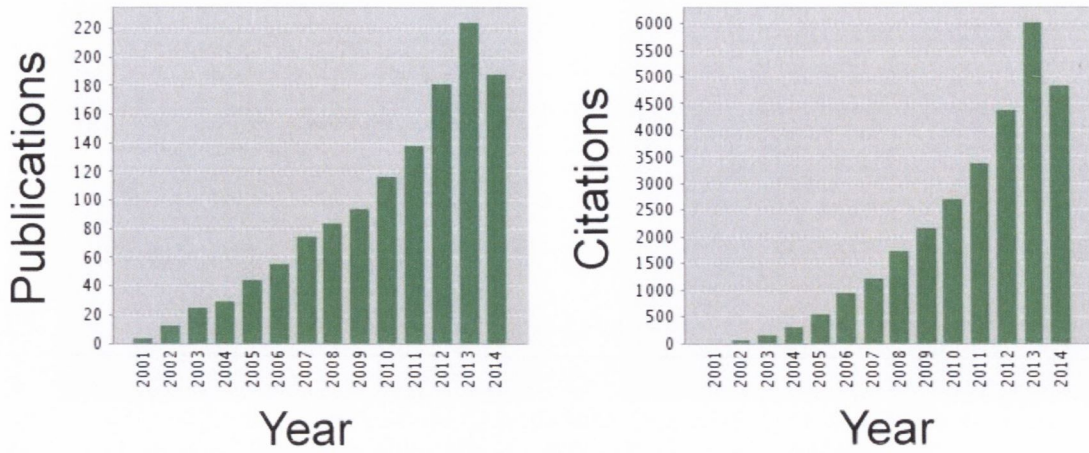
FIGURE 1.1. Plots illustrating the rise in publications and citations for the term "nanowire network" since 2001. Data downloaded from Thomson-Reuters Web of Science,[20] September 2014.

technologies,[14,21] the need to find a replacement for these TCOs grows. TCOs are typically very brittle materials, and show large increases in resistance under even very modest strains.[22] In addition, the cost of indium is on the rise as worldwide stocks begin to deplete,[21] making the current market leader, ITO, less and less commercially viable. It is therefore necessary to find a material which not only mirrors the impressive performance of TCOs in terms of transparency and conductivity, is capable of meeting the demands of future technologies such as flexibility, but which is also cheap and compatible with current large scale manufacturing methods.[23]

In order to meet industry requirements, a transparent conductor should demonstrate high conductivity, given by the sheet resistance, R_s, of less than $100\,\Omega/\square$, while maintaining high optical transmittance, T, of greater than 90%. While each application will have different requirements, this is a simple benchmark for which to aim. Thus far the highest performing materials have all been networks of nanomaterials, with Ag nanowires currently leading the field.[24] Figure 1.2 is a reproduction of a plot by De et al., comparing the performance of various nanomaterials (Ag and Cu nanowires, single-walled CNTs, and exfoliated graphene) in terms of optical transmittance and sheet resistance,[25] where the $T = 90\%$, $R_s < 100\,\Omega/\square$ region has been highlighted. It is clear that although none of the data shown crosses this region, Ag and Cu nanowire networks are the closest to approaching it. As such Ag nanowire networks have received quite a bit of attention, with many groups working on methods to improve the performance and meet these industry requirements.[26–31] Indeed, a number of companies have emerged in the past few years with Ag nanowire-based transparent ink technologies; one of these, Cambrios Technologies, claims sheet resistances below $50\,\Omega/\square$ at transmittance values of $\sim 98\%$ for its ClearOhm technology.[32]

A large factor determining the success of network materials and the research attention they have received is due to their excellent mechanical properties. Compared to ITO or FTO,
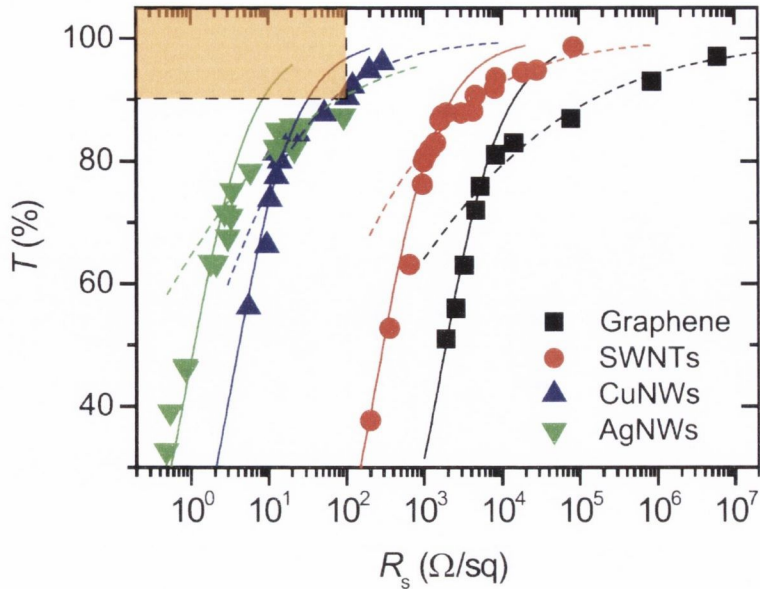
FIGURE 1.2. Plot of optical transmittance as a function of sheet resistance for a range of materials, including Ag and Cu nanowires, SWNTs, and exfoliated graphene. The region showing the industry required performance values of $T > 90\%$ and $R_s < 100\,\Omega/\square$ is highlighted. Modified from De, 2011.[25]

networks of Ag nanowires show remarkable stability under both compressive and tensile strains. Figure 1.3 shows the relative resistance change of ITO, FTO and Ag networks under repeated bending to a radius of 5 mm, demonstrated by Langley et al.[24] De et al. demonstrate this stability under both compressive and tensile bending on networks, and show almost no ($< 2\%$) change in resistance over 2000 bending cycles to a radius of 2.5 mm.[13] The stability of these networks to stretching has also been shown. Lee et al. demonstrate enormous tensile strains of over 450% with a relative resistance increase (R/R_0) of only 10, which then return to their initial resistance upon relaxation.[33] They achieve this remarkable result by utilising very long nanowires ($> 100\,\mu$m) and depositing them on pre-strained substrates, such that a low resistance is achieved even at very high strains. These impressive results help to illustrate why Ag nanowire networks are seen by many as the future of flexible, transparent conducting materials.

1.1.2 OPTIMISING NETWORKS

The fundamental unit of a nanowire network is the nanowire-nanowire junction, and it is the junction that ultimately determines the performance of the final film. If the junctions are highly resistive, this translates to a high sheet resistance of the film. Conversely, if the resistance of the junctions is very low, then the film properties are determined by a combination of contributions from both the junction as well as the nanowires themselves. It is generally assumed, however, that the junctions are the limiting factor in the resistance of a nanowire network. Indeed, Sorel et al. demonstrated by tuning the aspect ratio, L_{NW}/d_{NW},
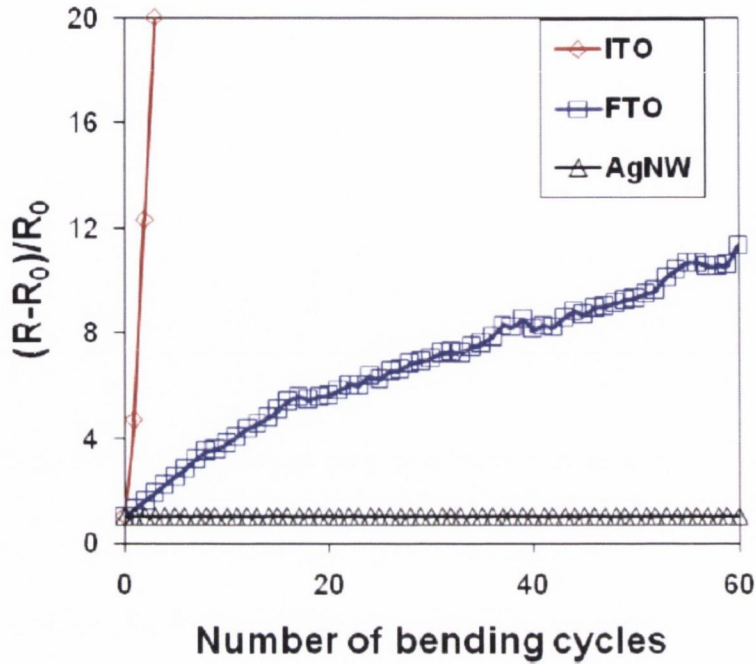
FIGURE 1.3. Plot showing the relative change in sheet resistance as a function of bending cycle for ITO, FTO and Ag nanowire films. Bending radius was 5 mm. Reproduced from Langley, 2013.[24]

of the nanowires – where L_{NW} is the nanowire length, and d_{NW} the nanowire diameter – that the sheet resistance could be optimised. They concluded that this is due to the presence of fewer junctions spanning the electrodes, thereby improving the conductivity.[34] There is therefore a large body of work dedicated to optimising the network properties through improving the junction properties. As will be explained in chapter 3, the Ag nanowire fabrication process results in a thin polymeric coating on the surface of the nanowires.[35] This coating, in its untreated state, will impede the flow of current and is therefore detrimental to the performance of any transparent conductor. It is therefore standard practice to apply a post-fabrication treatment to the network in order to remove this polymeric layer and fuse the nanowires together.

Thermal treatments, either on a hotplate or in an oven or furnace, are common and produce high quality networks,[13,36–38] although it has been shown that annealing for too long results in an increase in network resistance as the nanowires begin to melt and the connections break.[36,38] Mechanical pressure has also been shown to be a highly effective technique.[34,39] Tokuno et al. demonstrate that an as-formed, 3-D network treated to mechanical pressing up to 25 MPa is turned into a pseudo 2-D network as the junctions are compressed together, with a corresponding improvement in the conductivity of three orders of magnitude.[39] Another treatment shown to improve the network resistance was through exposure to high intensity white light. In their 2012 paper, Garnett et al. expose an as-formed network to a broadband tungsten-halogen lamp with a power density of

$30\,\mathrm{W\,cm^{-2}}$, demonstrating that this causes the nanowires to weld together at the junctions due to plasmonic excitation.[28] The results however show only a modest improvement in the network conductivity, demonstrating a relatively high resistance of $\sim 1\,\mathrm{k\Omega}$ post exposure. While this approach is novel, it has yet to be proven an effective method of optimising the sheet resistance compared to either mechanical or thermal treatments. A very recent study that appears to produce impressive results is reported by Zhu et al., where they expose a polymer-coated Ag nanowire network to a room temperature plasma.[40] Fourier transform Raman spectroscopy analysis indicated the complete removal of the polymer capping layer, and post-exposure measurements of the sheet resistance showed $\sim 50\,\Omega/\square$ at $T = 95\%$, making it one of the highest performing networks reported to date.

In each case, the improvement in sheet resistance is assumed to be a direct result of an improvement in the junction resistance; while this may be a reasonable assumption, it is only occasionally backed up by direct measurements of individual junctions. In 2010, Hu et al. published a study on the optimisation of Ag nanowire networks for transparent conductor applications by electrodepositing gold onto as-fabricated networks.[26] An improvement in the sheet resistance of two orders of magnitude was observed upon Au coating. 4-probe measurement of an individual junction was performed pre- and post-Au deposition, and it was found that the junction resistance, R_{jxn}, decreased from $>1\,\mathrm{G\Omega}$ to $450\,\Omega$ upon deposition of the Au. The enormous improvement in R_{jxn} was attributed to the formation of a Au shell surrounding the Ag nanowires. The study published by Garnett et al. in 2012 also performed measurements on single junctions to demonstrate the effect of the plasmonic welding.[28] They perform 2-probe electrical measurements pre- and post-exposure to the white light source, and demonstrate a significant reduction in the resistance measured. However, as no exact numbers are given in the paper, R_{jxn} could only be estimated from their results to be $\sim 10\,\mathrm{k\Omega}$. In 2014, Song et al. also performed a 2-probe resistance measurement on an individual Ag nanowire junction, measuring a value of $185\,\Omega$.[41] They estimate a resistance contribution from the nanowires of $180\,\Omega$, thereby implying a very low value for the junction resistance of less than $10\,\Omega$.

A number of attempts have also been made to extrapolate information regarding the junction resistance from experimental results of the bulk sheet resistance. Lee et al. published one such study in 2008.[36] They compute the sheet resistance of computer generated random meshes given the user defined parameters of nanowire length/diameter, nanowire resistance and junction resistance, as well as nanowire density. They find that experimental results of sheet resistance as a function of nanowire density may be approximated by simulating a range of R_{jxn} values from 1 to $100\,\Omega$, the upper values of which map onto lower nanowire densities, and vice versa. The reasoning given for this result is that at higher network densities the number of junctions per nanowire is greater than 1, and therefore the network chooses the lower resistance junctions. At lower densities it does not have this option and thus in this region R_{jxn} is more reflective of the average value. Mutiso et al. performed a much more comprehensive study in 2013, combining simulation of random 2-D rod networks with experimental sheet resistance measurements.[42] Modelling a network as

a quasi-2D random assembly of rods generated using a Monte Carlo process, and calculating the resistance of the subsequent films, they compare their simulated results to experimental sheet resistance data. In order to fit the data to the simulations, a single parameter was varied, namely the average junction resistance, R_{jxn}. They find that an R_{jxn} value between 1.5 kΩ and 2.5 kΩ is required to fit the experimental data most accurately. Additionally they simulate sheet resistance values as a function of nanowire aspect ratio, and find that performance improves with increasing aspect ratio, the highest measured being $L_{NW}/d_{NW} = 800$ – in agreement with the results of Sorel et al.

It is clear from these studies, where the junction resistance has been both experimentally measured and extrapolated based on bulk sheet resistance measurements, that there is an enormous variance in the values obtained. This variance highlights a fundamental lack of understanding regarding the contribution of the junction to the ultimate performance of the network. There is therefore a great need to perform a detailed study of individual nanowire junctions, in order to obtain a more complete understanding of these networks. This topic is addressed in chapter 3, where these previous studies are analysed in greater detail, and an in-depth experimental study of nanowire junctions is presented.

1.1.3 ALTERNATIVES TO Ag

Despite the attention they have received and the impressive performance that has been demonstrated in Ag networks, there remain some limitations to this material. For example, the high cost of Ag is expected to limit the use of Ag nanowire networks to only high value, niche applications. As such a substantial body of work has been developed looking at alternative metal nanowire networks. Having a resistivity only slightly higher (17 nΩ · m) than that of Ag (16 nΩ · m), but a tenth of the cost, Cu provides an interesting alternative from which to form metallic nanowire networks. In 2010, Wu et al. demonstrate the potential of Cu nanowire networks for transparent conductor applications.[43] Fabricating Cu nanowires through an electrospinning technique, they demonstrate extremely high performing networks showing 50 Ω/□ at 90% transmittance. In 2011, Rathmell et al. also demonstrate high performing Cu nanowire networks, employing polymer-coated nanowires as in the case of most Ag networks.[44] They demonstrate sheet resistances of < 50 Ω/□ at transmittance values of ~ 85%, comparable to results shown for Ag nanowire networks. Cu however, has a strong tendency to oxidise and therefore the performance of these films is likely to degrade over time. In a follow up paper, Rathmell et al. demonstrated this to be the case for both Cu and Ag networks. By storing the networks at 85 °C they show an order of magnitude increase in the resistance over 5 and 13 days, for Cu and Ag nanowire networks respectively.[45]

An additional issue faced by Cu nanowires is the undesirable red hue produced from these films. Next generation technologies will require accurate colour production, making tinted electrodes undesirable for many applications. In order to circumvent both of these issues, Rathmell et al. fabricated nanowires made of a cupro-nickel alloy. They demonstrate

that not only does this alloy show a remarkable resistance to oxidation at high temperature for only a modest increase in sheet resistance, but that the alloy also has a neutral grey hue, ideal for accurate colour production in advanced screen technologies.[45] Nanowire networks of inert noble metals, such as Au, offer another alternative to Ag or Cu if degradation is to be avoided.[46–48] Lyons et al. show excellent stability of their Au nanowire networks over time whilst demonstrating performances comparable to Ag ($49\,\Omega/\square$ at $T = 83\%$),[46] however the high cost of Au, in addition to the undesirable colouration makes the viable commercialisation of these materials rather unlikely. Chen et al. demonstrate another possible alternative by fabricating transparent-oxide coated Cu nanowires.[49] By coating a Cu nanowire network with elements such as Zn, Sn, or In, and then subsequently exposing them to an oxidising atmosphere, they demonstrate high performing networks ($29\,\Omega/\square$ at $T = 84\%$) that show excellent stability of the resistance at high temperatures. While they do not produce numbers comparable to those of the highest performing Ag networks, networks of this kind are ideal for applications that do not require extremely high transmittance/conductivity, but rather place focus on the lifetime of the technology.

Nanowire networks, with their combination of high conductivity, high transparency and impressive endurance under flexion appear to be the ideal candidate to replace ITO as the transparent conductor in future electronics. Networks may also be tweaked to produce properties that are ideal for certain applications, for example introducing thicker nanowires to increase haze and internal reflection for solar cell applications.[34] If networks are then to be designed to each specific application, a much greater understanding of the fundamental properties of the network is required. Specifically the contribution of the nanowire junctions to the properties and behaviour of the system must be better understood. The work presented in this thesis attempts to address this problem, as it is clear that there exists a fundamental lack of understanding regarding this most basic building block of networks.

1.2 NON-VOLATILE MEMORY

Electronic memory is ubiquitous. The average person living in a modern city will use up to five different forms of memory every day: FeRAM in smart-cards for public transport; flash memory in smart phones; volatile SRAM and DRAM on their PC; and finally a hard disk drive as the main non-volatile memory in most PCs. Society appears to have an ever-continuing thirst for more and more memory, and this trend is not expected to slow down any time soon. Each of these five technologies has its own advantages and disadvantages (read/write speed, power consumption, integration density, data retention, or bit cost) and so compromises must be made when choosing the best technology for a particular application. In addition to this, the semiconductor industry faces some big challenges as Moore's law (that the density of transistors on an integrated circuit chip doubles approximately every two years) approaches its physical limits. Complementary Metal-Oxide-Semiconductor (CMOS) field effect transistor (FET) based memory such as DRAM, SRAM, and flash (see Figure 1.4) are thus reaching their limit in terms of density. Dynamic random access memory (DRAM)
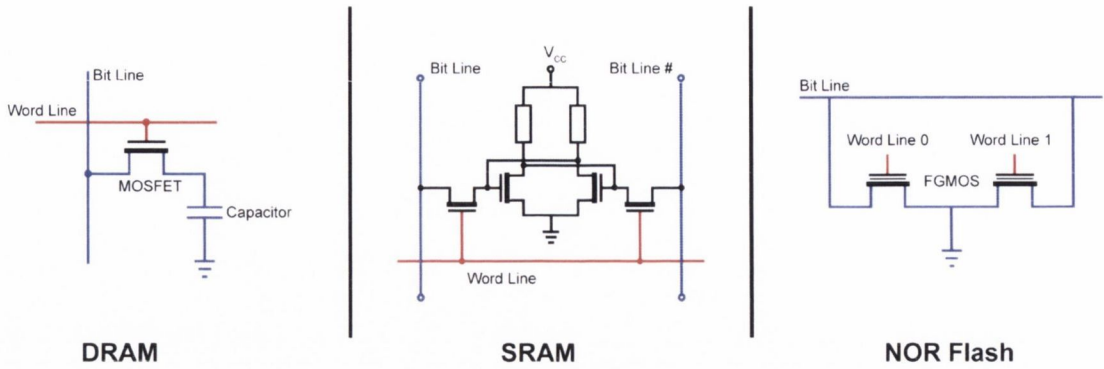
FIGURE 1.4. Memory cell architecture of DRAM, SRAM and flash memories.

consists of only one transistor and one capacitor, where the bit is stored as charge in the capacitor, and as such has a small bit footprint. However the stored charge leaks even under constant power, meaning the cell must be refreshed at periodic intervals. Static RAM (SRAM) has a much larger footprint, consisting of four to six transistors making a bistable flip-flop. Although still volatile memory, SRAM has much faster read/write times, lower power, and better static retention than DRAM. Flash memory operates via floating gate transistors (FGMOS), where the charge is stored in an electrically isolated, "floating" gate. Unlike DRAM or SRAM, flash is non-volatile, and the small footprint has led to the fabrication of extremely high bit densities, however its relatively slow write speed compared to SRAM makes it undesirable as a program memory.[50]

These challenges have led to a global effort aimed at developing a universal memory that will be the backbone of future electronics, comprising the best traits of all existing forms and which will be scalable into the future. Listed in Figure 1.5, numerous technologies have emerged in recent years as potential candidates for a universal memory. It is clear that a wide range of technologies exists, though only a small number show potential to be a viable universal memory. Of these, magnetoresistive RAM (MRAM) and phase change memory (PCM) are the most mature, and as such are described in the following section.

1.2.1 EMERGING NON-VOLATILE MEMORIES

MRAM has existed for almost two decades,[52] and in that time has received much praise for its potential as a universal memory.[53] Indeed several companies now produce MRAM chips for niche markets.[54] MRAM operates on the principle of a magnetic tunnel junction (see Figure 1.6(a)), whereby the tunnelling current between two ferromagnetic layers, separated by an insulating oxide, is modified by changing the magnetization of one layer with respect to the other. As a non-volatile memory, MRAM boasts a theoretically unlimited endurance as there are no components experiencing wear, as well as fast read/write speeds and excellent scaling potential – see table 1.1 for a comparison with other existing technologies.[50,51]

Phase change memory (PCM) has also received much attention as a potential universal memory.[55] Originally utilised in optical disc drives such as CDs, DVDs and Blu-rays, phase
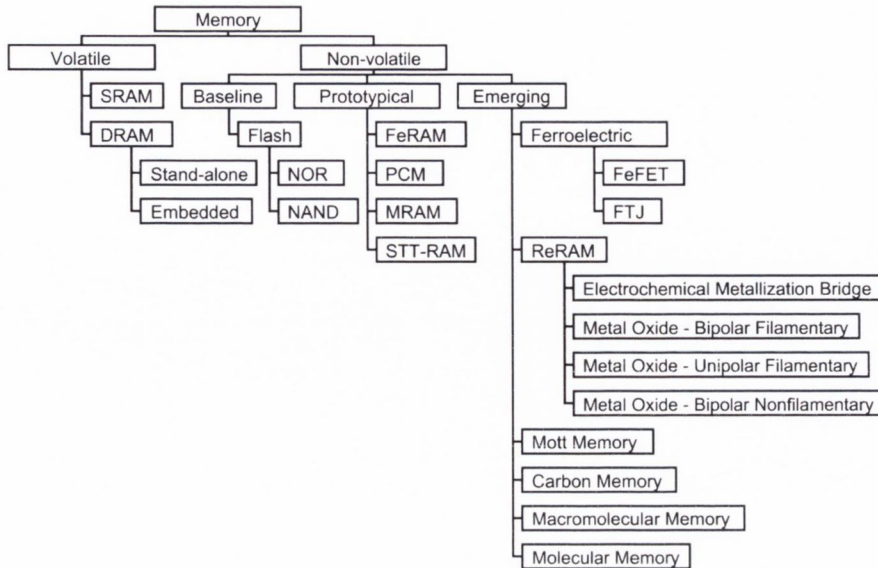
FIGURE 1.5. Taxonomy of established and emerging memory devices according to the International Technology Roadmap for Semiconductors (ITRS), 2013.[51]

change materials have been researched heavily for many years. With the decline of these technologies however, focus has shifted to developing non-volatile memories based on phase change materials such as GeTe, InSbTe, and $Ge_2Sb_2Te_5$.[56] PCM operates by inducing a phase change in these chalcogenide materials (crystalline to amorphous, or vice versa), and measuring the corresponding resistance change. The switching mechanism may be initiated by an electrical or an optical stimulus - hence their incorporation into optical drives. PCM boasts moderate to fast read speeds and excellent data retention, however the switching mechanism limits the write speed while also limiting the endurance (see table 1.1). The write energy per bit for both MRAM and PCM is also considerably higher compared to the CMOS based memories. For incorporation into demanding applications, these numbers must be reduced to prevent excessive battery usage and over-heating.

Although the physics behind these two technologies is very different, the basic architectures of both MRAM and PCM memory cells is quite similar. The active material – that which will store the bit – is sandwiched between two metal electrodes in a crossbar structure, as illustrated in Figure 1.6, where the electrodes are known as the bit line and word line respectively. In an array structure, leakage paths between neighbouring cells mean that each cell must contain an addressing device, usually a diode or a transistor, to ensure interaction with only the desired cell. This cross-bar structure enables very high planar densities, and allows for 3-D stacking to increase this even further. The crossbar architecture is one that has been adopted by other contenders in the universal memory race, most notably a class of redox-based resistance change memories, collectively classed as ReRAM. Although ReRAM is still classified by the International Technology Roadmap for Semiconductors (ITRS) as an emerging technology,[51] it has already demonstrated superb scalability, retention time, and write/erase speeds (see table 1.1). It is on this class of resistive switching devices that

TABLE 1.1. Comparison of established and emerging memory technologies

	DRAM	SRAM	NAND Flash	MRAM	PCM	ReRAM
Feature size	36 nm	45 nm	16 nm	65 nm	45 nm	5 nm
Read time	<10 ns	0.2 ns	0.1 ms	35 ns	12 ns	N/A
Write/Erase time	<10 ns	0.2 ns	1/0.1 ms	35 ns	100 ns	<1 ns
Retention time	64 ms	*	10 y	>10 y	>10 y	>10 y
Write Cycles	$>10^{16}$	$>10^{16}$	10^5	$>10^{12}$	10^9	10^{12}
Write voltage	2.5 V	1 V	15-20 V	3 V	1.8 V	1-3 V
Single cell write energy (J/bit)	4×10^{-15}	5×10^{-16}	4×10^{-16}	2.5×10^{-12}	6×10^{-12}	$<10^{-12}$

* State preserved as long as voltage is applied
All values taken from the 2013 International Technology Roadmap for Semiconductors report on emerging research devices.[51]

the next section focuses, as it forms the basis of many of the measurements and results presented in the subsequent chapters.

1.3 REDOX MEMORY – ReRAM

Redox based memory, or ReRAM, is a class of resistive switch whereby a metal-insulator-metal (MIM) structure undergoes a reversible reduction/oxidation reaction, producing two different resistance states of the insulating material, "I". The "M" may refer to any good electron conductor, usually a metal, but can also include non-metallic electron conductors.[58] The phenomenon was first demonstrated by T.W. Hickmott in 1962, when he observed hysteretic current-voltage (I-V) behaviour in an $Al/Al_2O_3/Au$ system.[59] Since then resistive switching[†] has been demonstrated in a wide range of different materials systems, including binary oxides, multinary oxides, chalcogenides, as well as organic materials,[60-65] though the phenomenon appears somewhat ubiquitous, having been recently demonstrated in a poly-Si/SiO_2/poly-Si system.[66] Binary transition metal oxides, in particular TiO_2 and NiO, have been studied in the greatest detail, with NiO being the material of most interest with respect to the work presented in this thesis. Demonstrating very good scaling, low power requirements, and excellent data retention, ReRAM is highly competitive with technologies such as MRAM and PCM, and shows significant potential as a universal memory (see table 1.1). However, inconsistency from device to device, and a lack of understanding about the switching mechanism, mean much work has still to be done to bring this technology to

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[†]In this thesis, the term "resistive switch" will refer solely to ReRAM. Although MRAM and PCM may also be described as resistive switches, the term is held almost exclusively for redox based RAM.
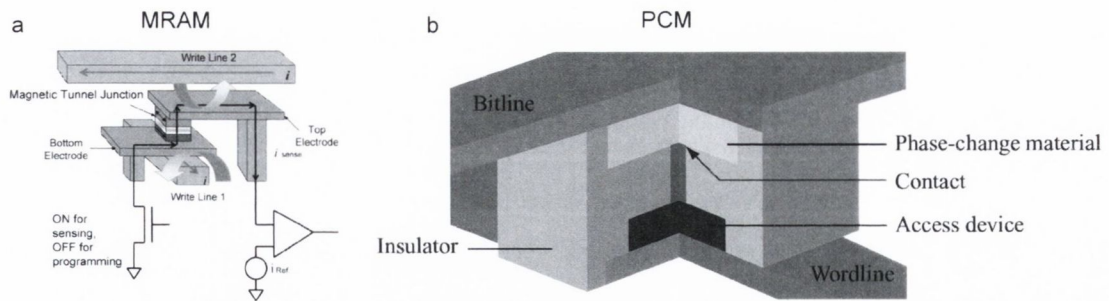
FIGURE 1.6. Basic memory cell architecture. Although both technologies operate via very different physics, the cell structure of both MRAM (a), and PCM (b) follows the same basic design. Large memory cell arrays are constructed of many perpendicular electrodes, known as bit lines and word lines (or write lines) respectively, allowing each cell to be addressed individually. An addressing device such as a diode or transistor is required to allow selection of the desired device. (a) reproduced from Engel, 2005.[57] (b) reproduced from Raoux, 2008.[55]

the market.[51] The following section introduces the various switching mechanisms, and latest research on ReRAM.

1.3.1 SWITCHING MECHANISMS

Resistive switching (ReRAM) devices have two stable resistance states: the low resistance state (LRS), and the high resistance state (HRS), and switching between these forms the basis of the memory effect. To program a device, also known as setting the device, a voltage, V_{SET}, is applied across the two electrodes inducing a redox reaction within the active layer and producing the LRS. This state is then erased, or reset, by applying a voltage, V_{RESET}, switching the state of the active layer to the HRS. This may then be cycled repeatedly, establishing the same LRS and HRS in each case. Prior to initial operation, a pristine device must undergo an electroforming process, whereby the LRS is established for the first time through the application of a voltage, V_{FORM}, which is typically much larger than V_{SET}.

ReRAM may be divided into two classes: bipolar – materials for which the resistance change is dependent upon the polarity of the applied voltage; and unipolar – materials for which the resistance change does not depend on the voltage polarity. This is illustrated in Figure 1.7. In unipolar devices, the forming and set events (depicted by red traces in Figure 1.7) may occur at both positive and negative polarity. A compliance current (CC) is set by the system electronics to limit the current during these steps and prevent unwanted switching events. Applying a voltage across the device in the LRS, current is driven through it (green trace, Figure 1.7) eventually switching the device back to the HRS. Bipolar device operation is dependent on both the magnitude and the direction of the applied field and is thus field driven, while unipolar devices depend only on the magnitude of the applied field and are controlled primarily by the current. The device may be set to the LRS once more by applying a field of sufficient magnitude.

Given the large number, and numerous types of materials (semiconducting, ionic etc.)
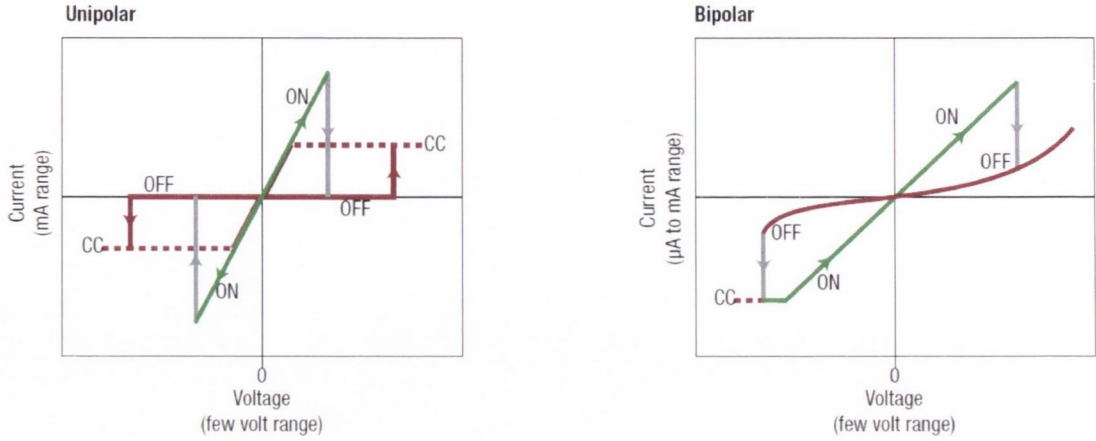
FIGURE 1.7. Unipolar and bipolar switching operation in MIM structures. Reproduced from Waser, 2007.[58]

that have displayed the resistive switching phenomenon, there are a variety of different mechanisms at play, and currently there is still significant debate as to the exact details of each. Determining the mode of operation, be it unipolar or bipolar, gives a first indication of what the mechanism might be. The details of and current research on the three main mechanisms is expanded upon in the following sections.

1.3.1.1 Electrochemical Metallization Memory

Electrochemical metallization (ECM) memory, also known as electrochemical bridge ReRAM or conductive bridge RAM, is a bipolar resistive switching mechanism first studied in the 1970s. A simple ECM cell design consists of an ion conductor sandwiched between two metal electrodes, as in Figure 1.8. One of the electrodes should be an electrochemically active material (usually Ag, or Cu), and is the active electrode (AE), while the opposing counter electrode (CE) should be electrochemically inert. While Pt is most commonly used, the CE may be any inert conductor.[67] The ion conductor, or solid electrolyte, should be a metallic ion (M^{z+}) conductor and may be one of many compounds, even those with relatively low ionic conductivity (e.g. SiO_2 or GeS_2). The first system to demonstrate the resistive switching effect, and resemble a modern ECM, was a Ag/Ag-doped As_2S_3/Mo thin film reported by Hirose and Hirose in 1976.[68] Numerous compounds have since demonstrated the effect, the most studied being the Ge_xS_y and Ge_xSe_y family of compounds.[67,69]

A schematic of the resistive switching mechanism in an ECM cell is depicted in Figure 1.8 for a cell with a Ag active electrode and Pt counter electrode. In the pristine state (Figure 1.8 (a)), the solid electrolyte is non-conducting, and thus the cell is in a HRS. Application of a positive bias on the active electrode results in the anodic dissolution of Ag into the solid electrolyte according to the following reaction:

$$Ag \rightarrow Ag^+ + e^-$$ (1.1)
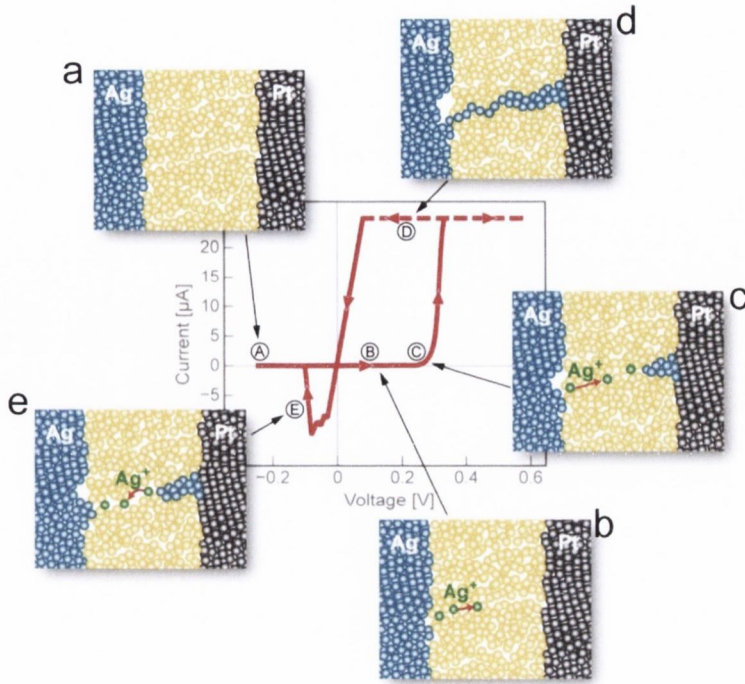
FIGURE 1.8. Operation of an electrochemical metallization cell. Application of a bias to the pristine device (a), results in the growth of a metallic Ag filament from the inert Pt counter electrode toward the Ag active electrode (b – d). Once the filament reaches the Ag active electrode the device is in the LRS. Bias of an opposite polarity causes the dissolution of the filament (e), and the device reverts back to the HRS. Reproduced from Valov, 2011.[67]

Under the action of the electric field, these metal ions drift to the counter electrode where they are reduced and Ag is electro-crystallized on the counter electrode (Figure 1.8 (b) and (c)) via the reaction:

$$Ag^+ + e^- \rightarrow Ag \tag{1.2}$$

The Ag filament grows preferentially from the CE to the AE via this electro-crystallization process. Once the metallic filament makes ohmic contact with the AE the LRS is established and the cell is programmed (Figure 1.8 (d)). The cell retains this programmed state until a negative bias of sufficient magnitude is applied to the AE, where the electro-crystallization process is reversed and the cell returns to the HRS. The voltage required to program the pristine cell is typically higher than that required in subsequent steps, and is thus considered an electroforming process.[67] Though it has not yet been experimentally confirmed, the filamentary model is widely held as the primary mode of operation in ECM cells. Some recent results, while not direct evidence in themselves, do point to it as the mechanism at play, and are discussed below.

Kund et al. reported on a $Ag/Ge_xSe_y/W$ cell that showed no dependence of the LRS resistance with device area, down to 20 nm.[70] Kim et al. demonstrate a similar result in a $Cu/Cu_2S/Ti$ cell, although the smallest cell measured in that study was only 2 μm.[71]
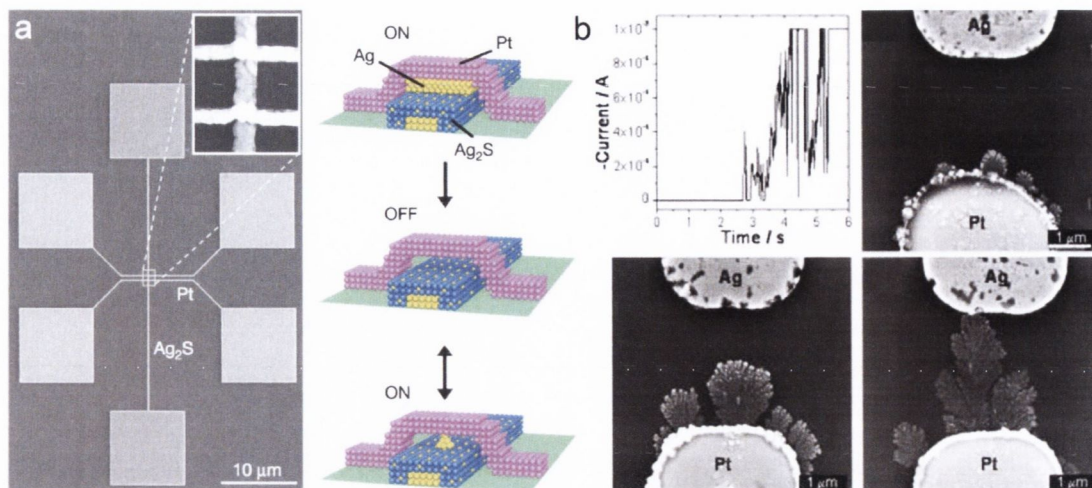
FIGURE 1.9. Electrochemical metallization memories (a) Quantized conductance atomic switch (QCAS) in a $Ag/Ag_2S/Pt$ cell. Reproduced from Terabe, 2005.[72] (b) Visualisation of Ag dendrites forming between planar Ag and Pt electrodes. Reproduced from Guo, 2007.[73]

These results indicate that the LRS is produced as a result of a spatially localised event, and a metallic filament is consistent with this description. Indeed, in 2005 Terabe et al. demonstrated quantized conductance in a $Ag/Ag_2S/Pt$ ECM cell, in what they call a quantized conductance atomic switch (QCAS) – see Figure 1.9(a). They showed that the conductance of the LRS was quantized with a unit of $2e^2/h$, where e is the electron charge and h is Planck's constant. This can only occur if the width of the conducting channel is on the order of the Fermi wavelength for Ag (0.52 nm),[72] again strongly indicating the action of a localized filament. Visualisation of the switching mechanism in vertical ECM cells has yet to be achieved, though interesting results on planar systems have been reported. Guo et al. demonstrated bipolar switching in a planar cell consisting of Ag and Pt planar electrodes bridged by a small volume of deionised water. Upon examining the cell post set and reset events, the presence of Ag filaments was clear (see Figure 1.9(b)), again strengthening the filamentary hypothesis.

While a number of challenges have thus far prevented its emergence as a competitive memory, most notably switching uniformity and poor write/erase speed, very promising qualities have been demonstrated in ECM cells. As explained above, the LRS shows no dependence on the device size, indicating that it may be possible to scale the cell size down to very small values without loss of performance. In addition to this, high endurance rates have been shown. Aratani et al. demonstrated 10^7 write/read/erase cycles in a Cu-Te/GdO_x/W system,[74] and Kozicki et al. demonstrated 10^{10} cycles in a Ag/Ag-doped Ge_xSe_y/Ni cell. While these numbers do not compare with those of SRAM ($>10^{16}$),[51] ECM based memory could however replace flash memory in future applications. Finally, cell design and fabrication requirements, such as the use of W counter electrodes, align well with existing CMOS technology, and allow for relatively straight forward incorporation into CMOS fabrication processes.[70] ECM memory therefore shows great potential as a

future universal memory technology, though several challenges remain before integrated ECM based RAM technology can be realised.

1.3.1.2 Bipolar Metal Oxide ReRAM

The resistive switching of transition metal oxides (TMOs) is currently a topic of intense scientific research, and there exists significant debate within the community as to what the exact physical mechanisms are. The controversy stems largely from the fact that multiple mechanisms appear to be at work, with multiple materials systems displaying both bipolar and unipolar switching.[75–77] This section focuses on the bipolar switching behaviour in TMOs, and will attempt to summarise the recent advances in this area.

Bipolar resistive switching in metal oxides has been studied since the late 1960s,[78] and since then has been demonstrated in a wide range of binary and multinary oxides, including TiO_x,[79] TaO_x,[80] HfO_x,[81] AlO_x,[82] WO_x,[83] and $SrTiO_x$.[84] The stoichiometry of these materials tends to be such that they are oxygen deficient, and the mobile charged vacancies, $V_O^{\bullet\bullet}$ (in the Kröger-Vink notation), are proposed as the main charge carriers in the LRS. As in the case of ECM memory, bipolar TMO memory cells must contain some asymmetry. While this is often done by using different electrode materials, asymmetry may also be built into the cell by incorporating regions of higher defect density into the active switching layer.[85] Remarkable progress has been made in this field in the past few years, with research focused on TaO_x and HfO_x leading this advance. In 2012, Panasonic demonstrated an 8 Mb TaO_x ReRAM device with a write pulse speed of 8.2 ns,[86] and in 2013 Toshiba released details of a 32 Gb ReRAM memory integrated with 24 nm CMOS, though they did not release details of the materials used.[87] As the prototypical resistive switching TMO, TiO_2 has been extensively researched over the past decade, and as such in the following discussion of the bipolar switching mechanism in TMOs, this is where the focus shall be placed.

Figure 1.10(c) demonstrates the bipolar switching of a $Pt/TiO_2/Pt$ memory cell.[85] Sweeping to negative bias switches the device from a HRS to a LRS, producing an ON/OFF conductance ratio of $\sim 10^3$. Sweeping in the positive direction reverses this in a very well controlled manner. As in the case of ECM memory, an electroforming step must be carried out to produce the LRS for the first time. The polarity of the sweep during the initial electroforming step is not important, however the magnitude of the compliance current used is of critical importance to the resulting switching behaviour.[75,88] Yang et al. propose that this behaviour is due to the movement of positively charged oxygen vacancies, $V_O^{\bullet\bullet}$, generated at the anode interface according to the following equation.[85,89]

$$O_O{}^\times \rightarrow V_O^{\bullet\bullet} + 2e^- + \frac{1}{2}O_2 \qquad (1.3)$$

They find that the rectifying behaviour observed in the pristine state (Figure 1.10(b)) indicates the presence of a high concentration of oxygen vacancy defects (TiO_{2-x}) at the anodic interface, producing the asymmetry needed for bipolar switching. Under the action of the electric field, these mobile defects drift to the negatively charged top electrode creating
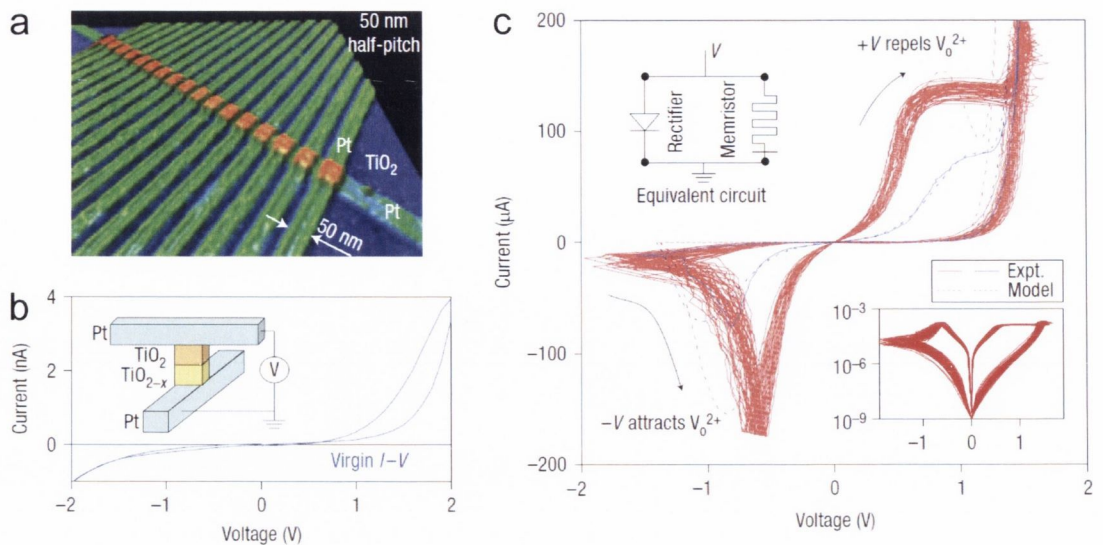
FIGURE 1.10. Bipolar switching in TiO$_2$ thin film devices. (a) AFM image of Pt/TiO$_2$/Pt crossbar ReRAM device. (b) Schematic of crossbar device illustrating device asymmetry through the use of TiO$_2$ and oxygen depleted TiO$_{2-x}$ regions within the film. (c) I-V curves showing bipolar switching behaviour. Reproduced from Yang, 2008.[85]

channels of high conductivity. Once they reach the top electrode, the metal-semiconductor Schottky barrier is broken down and the device is programmed to the LRS (Figure 1.10(c)). Once the polarity is reversed, the conducting vacancies are repelled from the top electrode and the barrier is re-established. A common trend among bipolar TMO resistive switches is the low switching current, usually tens or hundreds of microamperes.[81,85,90] In TiO$_2$ films, where the device was allowed to reach higher operational currents, bipolar switching was removed completely, and only unipolar operation remained.[75] The possible mechanisms behind this are discussed in the following section.

The excellent scaling properties of bipolar TMO based RAM have been demonstrated in recent years, with both 10 nm and 8 nm HfO$_x$ devices being demonstrated.[91,92] In addition to this very low switching energies have been shown. The lowest to date was shown by Tsai et al., who fabricated an AlO$_x$ device with carbon nanotube electrodes, and estimated the switching energy to be in the range 0.1–10 fJ per bit – comparable with DRAM.[93] Despite the remarkable progress that has been made in this area, many challenges still remain. All resistance switching technologies (including ECM, and both unipolar and bipolar TMO RAM) suffer from large variability in the switching parameters, posing a major challenge to their incorporation in real world technologies. Much work is required to establish uniformity not just across multiple devices, but simply within individual cells as well. In one recent overview article, Prall et al. highlight this variation by showing a variability of 10^4 in the HRS current, overlapping the LRS distribution.[94] The origin of this variability is thought to be due to the filamentary nature of the switching, as each filament varies slightly with respect to the previous, producing different resistance levels. An additional challenge for bipolar TMO RAM as a universal memory is the fabrication of memory arrays with all of the

necessary high performance properties, as typically trade-offs must be made.[51] Ultimately, bipolar TMO based ReRAM technology is likely still some years away from a viable product.

1.3.1.3 Unipolar Metal Oxide ReRAM

Transition metal oxides also display unipolar, or polarity-independent, switching. Often referred to as thermochemical memory, the switching mechanism is thermally driven rather than electrically driven as in the bipolar case. The phenomenon was first described in 1964 by Gibbons and Beadle for thin NiO films, where they attributed the switching mechanism to the formation of Ni filaments within the insulating NiO matrix.[95] Numerous oxides have since been shown to exhibit thermochemical switching, with NiO_x, TiO_x, and HfO_x being perhaps the most studied to date. Recently, significant progress has been made towards integrating unipolar ReRAM into existing CMOS processes. Shen et al. demonstrate a $W/TiON/n^+$ Si ReRAM device in 29 nm CMOS with an endurance of 10^6 cycles,[96] while Chang et al. demonstrated 4 Mb embedded ReRAM in 65 nm CMOS.[97] These advances show promise for the future of TMO based ReRAM, however issues regarding variability and power requirements still hamper it as a viable technology.[51] In the context of this thesis, the mechanism for unipolar switching in NiO is of most significance, as it provides the physical basis for the phenomena observed in chapters 3 and 5, and it is here that the focus shall be placed.

Figure 1.11 schematically illustrates the unipolar switching mechanism in a Pt/NiO/Pt ReRAM cell. As with electrochemical ReRAM and bipolar TMO ReRAM, thermochemical memory requires an electroforming step where the conductive filament is formed for the first time. Shown in Figure 1.11, when a positive bias is applied to the top Pt electrode, positively charged Ni ions are created. NiO is a known p-type semiconductor where the majority carriers are Ni vacancies, however under an applied bias the redox reaction shown in equation (1.4) produces Ni interstitials ($Ni_i^{\bullet\bullet}$),[89] and these positively charged defects may drift/diffuse toward the cathode.

$$NiO \rightarrow Ni_i^{\bullet\bullet} + 2e^- + \frac{1}{2}O_2 \tag{1.4}$$

It is hypothesized that at high levels of $Ni_i^{\bullet\bullet}$ generation, hole injection at the anode induces Joule heating sufficient to cause the formation of metallic filaments,[89] as illustrated in Figure 1.11(a). Using x-ray photoelectron spectroscopy and transmission electron microscopy it has been observed that filaments of metallic Ni exist within the NiO matrix during the LRS, and that these filaments preferentially form at the grain boundaries.[98–100] As the filament grows from the anode, electric field enhancement further facilitates the thermochemical reaction, accelerating the filament growth. Once the filament bridges the electrodes, the LRS is established. This is observed in current-voltage measurements as a sudden rise in the current level corresponding to the sudden change in conductivity – see Figure 1.11 (c) black and blue circles.

The compliance current set by the external electronics plays an important role in the
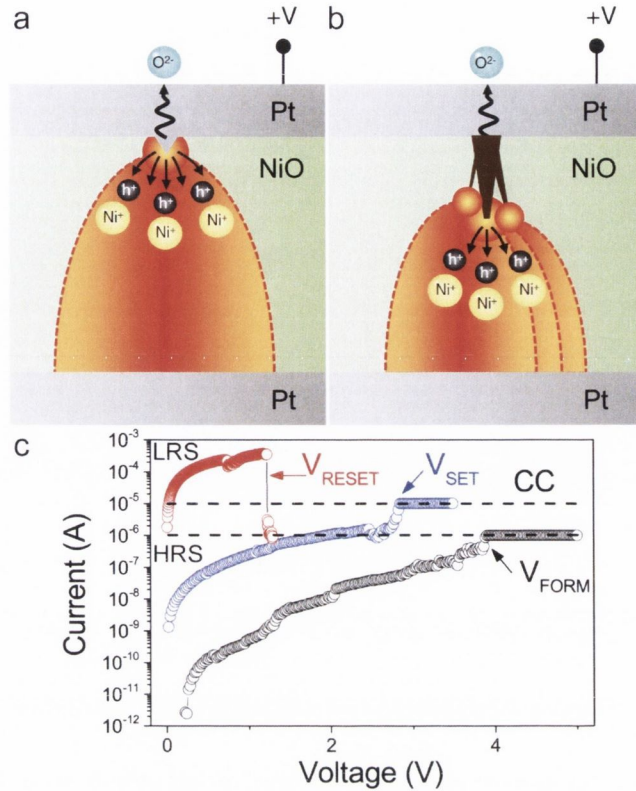
FIGURE 1.11. Resistive switching mechanism and electrical response in NiO. (a) Ni interstitial defects are formed via redox reaction at the anode in a Pt/NiO/Pt memory cell. Joule heating, caused by hole injection, causes metallic Ni to form within the NiO matrix. (b) The nucleation of Ni filaments causes an electric field enhancement resulting in an acceleration of the filament forming process. (c) I-V response of a unipolar ReRAM device. (a) and (b) have been reproduced from Kim, 2011.[89]

properties of the memory cell, as it determines the "'strength" of the conductive filament. The sudden increase in current flow upon establishing a metallic connection induces a large amount of Joule heating, causing the filament area to grow.[89] Indeed, in 1964 Gibbons and Beadle observed that if too much current is allowed to flow, irreversible breakdown of the oxide is observed.[95] Conversely, if the compliance current is set too low, then volatile switching, known as threshold switching, may occur. This is thought to be due to the formation of thin filaments which are unstable at zero bias.[63,101] As mentioned in section 1.3.1.2, unipolar switching has also been observed in TiO_2 systems. This transition from a bipolar to a unipolar mechanism is caused by the thermally assisted phase change to the metallic Magnéli phase (Ti_nO_{2n-1}, where $n = 3 - 9$) as the compliance current is increased.[89,102] It has also been shown for both TiO_2 and NiO films that the switching power has a direct correlation with the compliance current,[103,104] implying a thickening of the filament with higher current levels, consistent with that observed by Gibbons and Beadle.

The unipolar nature of the switching in materials such as NiO and TiO_2 implies the mechanism must not be an electrically activated drift, but rather a thermally activated

one, triggered by Joule heating within the conductive filament.[89] This has led to unipolar switching often being described as the fuse/anti-fuse mechanism, as the reset mechanism resembles the action of a simple household fuse.[58] Figure 1.11(c, red curve) shows the current-voltage trace for a reset event. The sharp transition at V_{RESET} is a trade mark of unipolar devices, and multiple models have been developed to describe this reset process. Russo et al. propose a self-accelerated dissolution of the filament via thermally assisted diffusion.[105] In this model, the Joule heating resulting from the large current densities within the nanoscale filament causes the conducting particles, most likely Ni atoms, to diffuse away from the filament. This thinning of the filament results in a further enhancement of the effect due to the increase in Joule heating, and accounts for the rapid increase in resistance seen in Figure 1.11. Chen et al. however propose a very different mechanism.[106] In their model, $V_O^{\bullet\bullet}$ defects are the primary component of the conductive filament, and the thermally assisted decomposition of Ni_2O_3 within the largely NiO matrix releases O^{2-} ions which recombine with $V_O^{\bullet\bullet}$ to dissolve the conductive filament. Although the model appears to account for the observed data, Ni interstitials have been shown to be the majority carrier in NiO, and make a conductive filament composed of $V_O^{\bullet\bullet}$ unlikely. Additionally, Lee et al. propose a model where the LRS is composed of multiple metallic filaments/pathways, which appears to account for the behaviour seen by Chen et al.[107] Thus, it is now largely accepted that the conductive filament is disrupted through a Joule heating induced, thermally activated event, though work still remains to conclusively determine the mechanism.

As mentioned previously, good progress has been made in developing unipolar TMO based ReRAM technology. It has been shown to be CMOS compatible, has demonstrated good endurance, switching speeds as fast as 5 ns,[108] and, due to the filamentary nature of the switching, promises to be highly scalable. Unipolar operation also enables the use of simple diode select devices which may be stacked vertically for higher density architectures, as well as simplifying circuit design. However, one of the major challenges facing unipolar ReRAM is the high switching currents required.[51] Unipolar devices typically show high ON/OFF current ratios, however this carries with it an inherently high reset current, which is not ideal for device application. While reset currents in the $100\,\mu A$ region have been demonstrated,[96,109] most devices still require hundreds of microamps or milliamps, while values of tens of microamps are ideal for device integration.[51] One recent paper by Chien et al. used a $TiN/WO_x/W$ stack, where the WO_x is the switching layer. It was demonstrated that by passing current laterally across the TiN top electrode, the Joule heating induced a resetting of the active layer.[110] An approach such as this may provide the solution.

Redox based resistive switching memory technology shows great potential to become a universal memory. While large variation in switching parameters and high reset currents continue to hamper the development of commercial products, it is only a matter of time before these barriers are overcome given the continuing rise in publications in this field. Excellent scalability, fast write/erase times, low write voltages and good endurance levels place ReRAM in a highly competitive position compared to other emerging non-volatile memories such as MRAM. As the prototypical resistive switch, NiO has been extensively

studied and is known to operate as both a unipolar and bipolar switch,[111] as well as exhibiting both memory and threshold switching responses. The resistive switching properties of this material are utilised in chapters 3 and 5, by taking advantage of the natural oxidation properties of Ni to form thin NiO passivation layers on Ni nanowires. The following section introduces nanowire based memory in order to provide a background to the results presented in these chapters.

1.4 NANOWIRE MEMORY

The ultimate scaling limits of RAM technology are currently defined by the limits of the various lithographic methods used to fabricate them; currently at the 14 nm node, scaling to the 10 nm node and beyond will be extremely challenging, and may limit the scaling of non-volatile memory if lithographic limits cannot be overcome.[51,112] One approach to overcome this scaling limit is to utilise the bottom-up approach and employ nanomaterials such as nanowires whose size is controlled through the growth process, and not by lithographic means. In the past several years a number of studies have taken this approach, demonstrating memory in nanowire structures. This section focuses on this work.

1.4.1 RESISTIVE SWITCHING IN METAL-OXIDE NANOWIRE STRUCTURES

The first study demonstrating non-volatile switching in nanowires was published by Kim et al. in 2008 – see Figure 1.12(a) and (b).[113] For this study they fabricated nanowires of NiO by electrodepositing Ni into nanoporous membranes of anodised aluminium oxide (AAO), and then subsequently thermally oxidised them to produce nanowires of NiO, approximately 70 nm in diameter. Depositing on an SiO_2 substrate and contacting with Ti/Au electrodes, they demonstrate electroforming of the device with only 2.5 V. This was a surprising result, as the long device length ($\sim 1\,\mu m$) would suggest much larger forming voltages. It was concluded that this was a result of the large grain sizes, which were of comparable size to the nanowire diameter. Grain size is known to have a significant impact on the switching characteristics due to preferential formation of conductive filaments at the grain boundaries.[99] Subsequent cycling of the device demonstrated unipolar resistive switching, displaying V_{RESET} and I_{RESET} values of 0.5 V and 230 μA respectively, comparable with the planar devices discussed in section 1.3.

Oka et al. also demonstrate the occurrence of resistive switching in NiO nanowire structures.[76,115] Rather than Ni nanowires, they fabricate heterostructured nanowires through laser ablation, forming an MgO/NiO core-shell structure (10 nm MgO core diameter and 10 nm NiO shell thickness). Contacted by planar Pt electrodes with an inter-electrode gap of only 300 nm, they observe bipolar switching behaviour. Despite showing very high switching voltages, in the range 10–15 V for both V_{SET} and V_{RESET}, the switching currents were very low, on the order of 10 nA. The bipolar behaviour was attributed to a cation
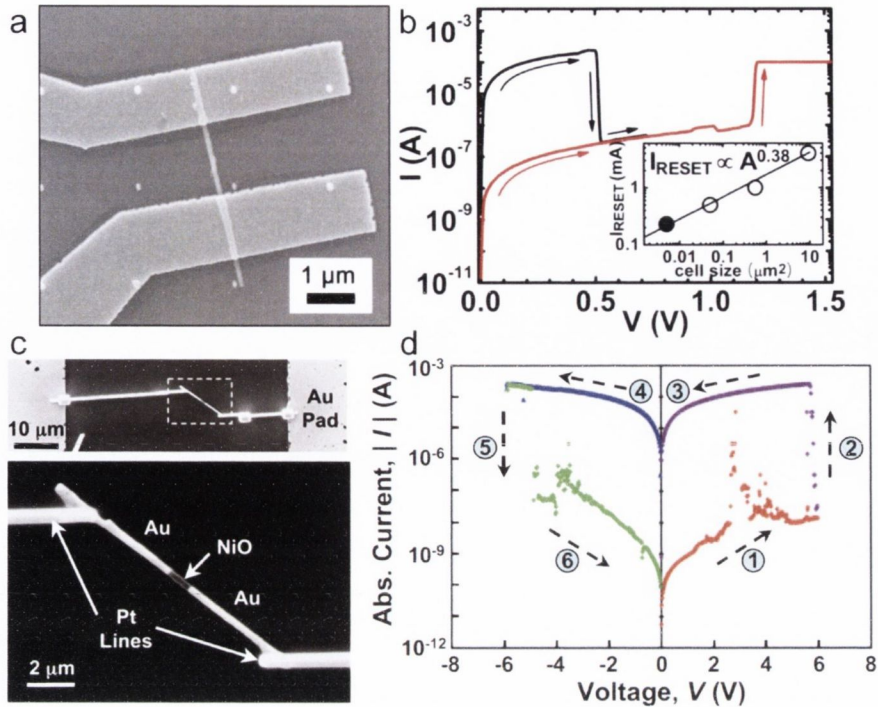
FIGURE 1.12. Resistive switching in single nanowires. (a) A single NiO nanowire contacted with two Ti/Au electrodes demonstrates unipolar resistive switching (b). Reproduced from Kim, 2008.[113] (c) Segmented Au-NiO-Au nanowire contacted with two Pt lines demonstrates bipolar resistive switching with high switching currents (d). Reproduced from Herderick, 2009.[114]

dominated LRS, in comparison to the metallic LRS that determines the unipolar behaviour normally observed in NiO. This behaviour was likely observed for two reasons: firstly the single crystal nature of the NiO would impede the formation of a conductive filament due to a lack of grain boundaries, and secondly the low switching currents observed would limit the Joule heating effect, known to cause a transition from bipolar to unipolar switching in TiO_2 systems.[75] By driving the system to higher currents, it may be possible to convert the switching behaviour to a unipolar response.

A novel approach to fabricating nanowire resistive switches was demonstrated by Tresback et al., and in a follow up paper by Herderick et al.[114,116] They form segmented Au-NiO-Au nanowires through a multi-step electrodeposition process into nanoporous AAO membranes. To fabricate these heterostructured nanowires, they first deposit a thick ($3\,\mu m$) layer of Au, followed by a thin ($900\,nm$) layer of Ni which is then capped with a final layer of Au. Subsequent thermal oxidation converted the Ni to NiO, thereby creating the MIM structure required for resistive switching. Despite using relatively high switching currents ($100\,\mu A$), bipolar switching was still observed – see Figure 1.12(c) and (d). This was attributed to a higher concentration of oxygen vacancy defects in the thermally oxidised NiO, creating a metal-oxide interface that could be controlled through the action of an electric field by changing the defect profile through the oxide. A subsequent study showed a re-

duction of the forming voltage by reducing the thickness of the NiO layer to 33 nm.[117] It is interesting to note from these comparative studies demonstrating both unipolar and bipolar behaviour, that unipolar switching demonstrates the more favourable combination of switching parameters – V_{RESET}, V_{SET}, and I_{RESET} – despite the generally high currents required for unipolar switching.

1.4.2 RESISTIVE SWITCHING IN CORE-SHELL NANOWIRE STRUCTURES

For the nanowire memories described above, the thickness of the active switching layer must be carefully defined, through either lithographic means or by carefully controlling the deposition of the oxide. Reducing the thickness to < 10 nm then becomes quite challenging. An alternative approach is to utilise core/shell nanowires where the metallic core acts as an electrode while the shell is the active switching layer. The obvious benefit of such an approach is a much greater control over the switching layer thickness, making sub 10 nm thicknesses feasible. The first study demonstrating switching in core/shell nanowires was published by Dong et al. in 2008.[118] Bipolar switching was demonstrated in single crystal Si – amorphous Si (a-Si) core-shell nanowires contacted with Ag electrodes. The nanowires were fabricated through successive metal-catalysed CVD steps at 435 °C and 450 °C to form the Si core and a-Si shell respectively, where the thickness of the a-Si layer was ∼ 5 nm. The bipolar switching was attributed to an electrochemical metallization mechanism, as Ag ions migrate through the thin a-Si layer forming a conductive filament. This argument was strengthened by investigating the switching behaviour as a function of temperature. It was found that the LRS was much more stable under reverse bias at low temperatures, pointing to a thermally-activated, diffusion-controlled model.

He et al. published a study in 2011 demonstrating unipolar switching in Ni/NiO core-shell nanowires.[119] Fabricated through electrodeposition into nanoporous AAO, the Ni nanowires were deposited onto SiO_2 substrates and immediately contacted with thin Au electrodes (Figure 1.13(a) and (b)). By allowing the nanowires to naturally oxidise in air, a thin, self-limited NiO layer was formed on the surface, which was subsequently contacted with an additional Au electrode. In this way they limit the thickness of the oxide to a single layer, approximately 4.5 nm thick. Setting a relatively high compliance current of 100 μA, unipolar memory switching was observed with V_{SET} values of ∼ 1 V, and I_{RESET} values of approximately 200 μA (exact figure not given) – Figure 1.13(d, black and blue traces). Interestingly, by adjusting the compliance current to lower values (∼ 10 μA), they are able to switch between threshold and memory switching (Figure 1.13(d, red trace)). This demonstration of both threshold and memory behaviour, indicates that it may thus be possible to fabricate novel switch / select-device circuits using core-shell nanowires, thereby lowering the footprint per bit even further.[120] The low V_{SET} and V_{RESET} values reflect the extremely thin nature of the active switching layer, which further highlights the benefits of using naturally occurring core-shell structures such as these.
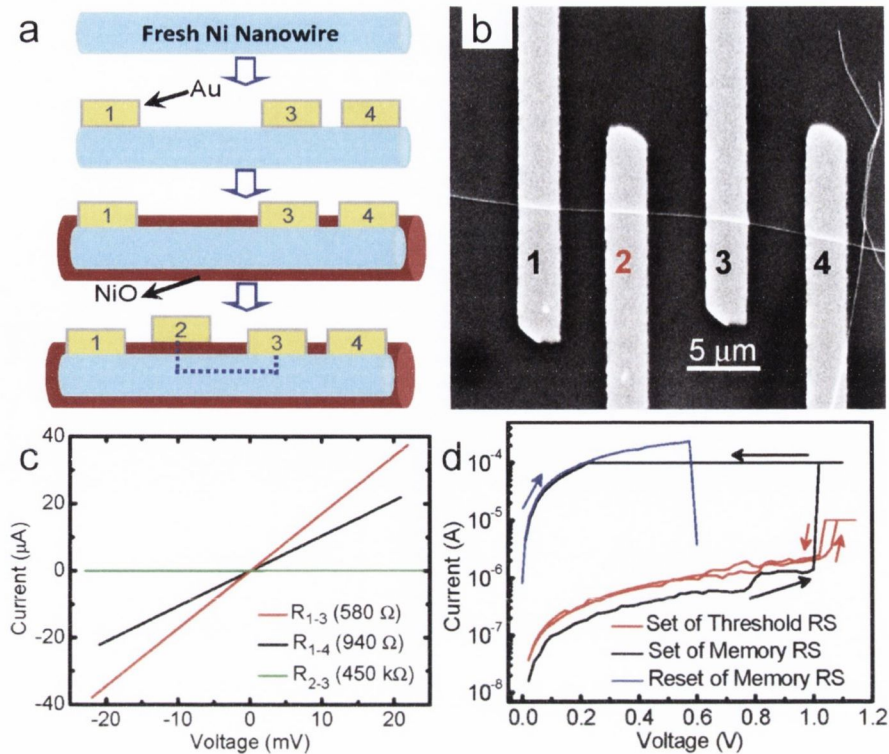
FIGURE 1.13. Unipolar switching in Ni/NiO core-shell nanowires. (a) Schematic of fabrication procedure used by He et al. Ni nanowires are contacted with Au electrodes (1,3, and 4) and allowed to oxidise naturally prior to deposition of a fourth electrode (2). (b) SEM image of Ni nanowire with four Au contact electrodes. (c) I-V curves showing ohmic contact of electrodes 1-3 and 1-4 with the Ni core. Electrodes 2-3 show a HRS due to the presence of the NiO. (d) Electrodes 2-3 show unipolar RS characteristics of the NiO shell, demonstrating both threshold and memory switching. Reproduced from He et al.[119]

1.4.3 CROSSBAR NANOWIRE MEMORY

The final nanowire-based memory structure that will be looked at here, and perhaps the one with the greatest scaling potential, is that of crossbar nanowire memory. As in Figure 1.14(a), two crossed core-shell nanowires naturally create a metal-oxide-metal structure, with the nanowire cores acting as the metal electrodes, which should then act as a memory cell. In 2011, Cagli et al. demonstrated this to be the case for crossed Ni/NiO core-shell nanowires, as in the work by He et al.[121] To aid the fabrication of crossed wires, they employ an elegant magnetic alignment technique, taking advantage of the ferromagnetic properties of Ni, by depositing nanowires onto a SiO_2 substrate via a drop-casting method in the presence of a magnetic field. For subsequent nanowire depositions, the sample was reoriented relative to the magnetic field, forming highly aligned, perpendicular crossbar nanowire structures as shown in Figure 1.14(b) and (c). Each nanowire was then contacted with Au electrodes at both ends in order to perform 2-probe resistance measurements on the individual nanowires.

By applying a bias across the junction via the electrodes contacting each nanowire (A and B, in Figure 1.14(b)), repeatable unipolar resistive switching was demonstrated, as
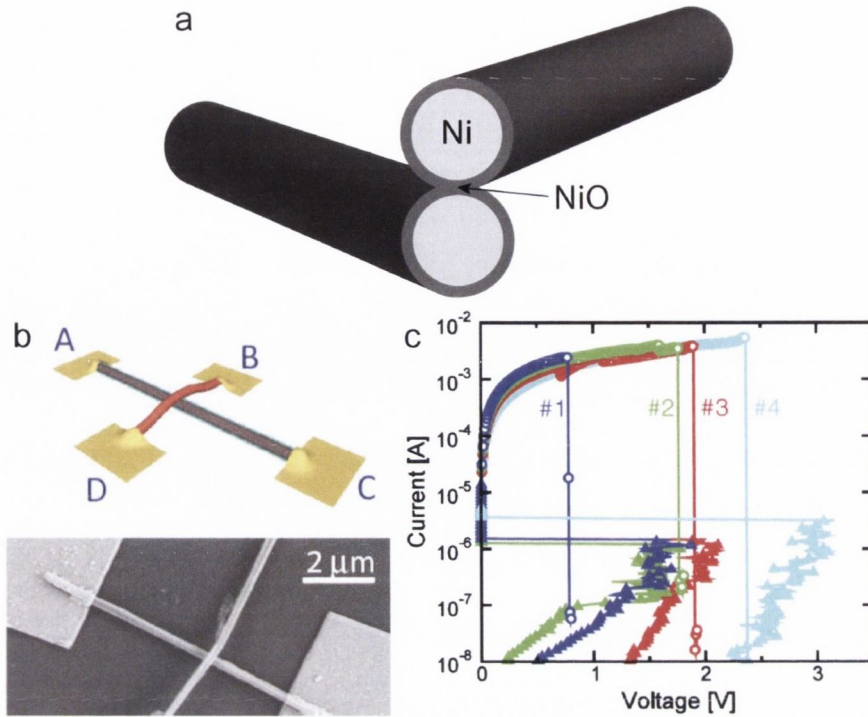
FIGURE 1.14. Demonstration of memory in a core-shell nanowire crossbar structure. (a) Ni/NiO core-shell nanowires fabricated in a crossbar structure and contacted with Au electrodes, and (b) SEM image showing the crossbar structure. (c) Unipolar resistive switching is demonstrated in this crossbar structure. I-V curves show sequential cycles of the device. Adapted from Cagli, 2011.[121]

shown by the current-voltage curves in Figure 1.14(c). By monitoring the resistance of each nanowire via the two contacting electrodes, it was verified that the switching behaviour observed did not occur at the nanowire-Au interface, and therefore occurred only at the nanowire junction. The resistance across the nanowire junction was measured to be 265 Ω in the LRS, and 16 MΩ in the HRS. This is a very important result, as it demonstrates that a single nanowire junction may act as a resistive switch, and is therefore extremely relevant in the context of this thesis. Extending the results obtained for a single junction, the authors envisage a full nanowire crossbar array, with a 20 nm cell-cell pitch corresponding to the 10 nm technology node.[51] If such a design were to be achieved, the theoretical memory density is calculated to be as high as 0.25 Tb cm^{-2}. Though currently beyond the capabilities of current fabrication techniques, these claims are somewhat justified based on the work of Whang et al., who previously demonstrated the fabrication of highly aligned, perpendicular nanowire crossbar arrays over centimetre scales.[122]

Nanowire memory presents an exciting alternative to conventional planar RAM devices, particularly as the challenges associated with scaling beyond 10 nm become an issue. Utilising the thin, naturally forming oxide of materials such as Ni, the switching parameters can be reduced to levels favourable for current integration technologies. In particular, if crossbar nanowire arrays can be realised, the opportunity is there to fabricate both memory and

select-device elements from a single material, potentially reducing the bit size considerably and enabling extremely high density non-volatile memory arrays. However, as was stated at the top of this chapter, the reliable placement of nanomaterials poses a significant barrier to the commercial realisation of this technology. The results of He et al. and Cagli et al. are drawn upon in chapters 3 and 5 as the properties of Ni/NiO core-shell nanowires are examined in the context of both single junctions and much larger networks, where the facile fabrication of nanowire network-based resistive switches is shown, thereby circumventing the issues associated with nanowire placement.

1.5 NEUROMORPHIC NETWORK SYSTEMS

The final section in this chapter combines the concepts of nanowire networks and resistive switching discussed thus far to describe the work on neuromorphic network systems. Although still a very new field, work in this area has the potential to revolutionise the standard computing paradigm and realise Turing's B-type unorganised machine.[123] First reported by Stieg et al. in 2012, they fabricated networks of highly interconnected Ag nanostructures with bipolar junctions, dubbed neuromorphic networks, and demonstrate interesting phenomena such as soft and hard memristance, and cross-correlation of the switching behaviour for adjacent networks.[124]

The quantized conductance atomic switch, first demonstrated by Terabe et al., was described in section 1.3.1.1.[72] Fabricated as a $Ag/Ag_2S/Ag/Pt$ cell, a positive bias on the Pt electrode switches the cell to the HRS. Subsequent cycling of the bias polarity results in a Ag atomic bridge spanning the 1 nm gap, exhibiting the quantized conductance of $2e^2/h$. Stieg et al. fabricate networks of atomic switches by sulfurizing complex, interconnected networks of Ag. They claim that exposing as-fabricated networks to sulfur gas at 150 °C creates network junctions composed of Ag_2S, though it is not clear that the nanowire length does not also become sulfurized. The networks themselves are fabricated through an electroless deposition of dendritic Ag filaments onto a dense array of Cu seed posts (Figure 1.15(a)). The resulting structure is a complex, 3-D network of interconnected nanoscale Ag wires, shown in Figure 1.15(b).

It was shown that applying a sufficient bias across the sulfurized network resulted in a change in the network resistance. Subsequent voltage sweeps showed pinched hysteresis loops in the current response (Figure 1.15(c)), akin to the behaviour of bipolar resistive switching. This was a clear demonstration that the sulfurization had indeed modified the network, resulting in a resistive switching behaviour reminiscent of a single device despite the presence of many junctions. Using ultrasensitive IR imaging to map areas of Joule heating in the network (Figure 1.15(d)), the conductance was shown to be distributed across the entire network rather than through narrow channels of connected wires. This analysis does not however clearly show that the resistive switching response is a contribution from the entire network, but rather shows that the entire network takes part in conduction. It was also shown that the conductance states of the network demonstrated only temporary
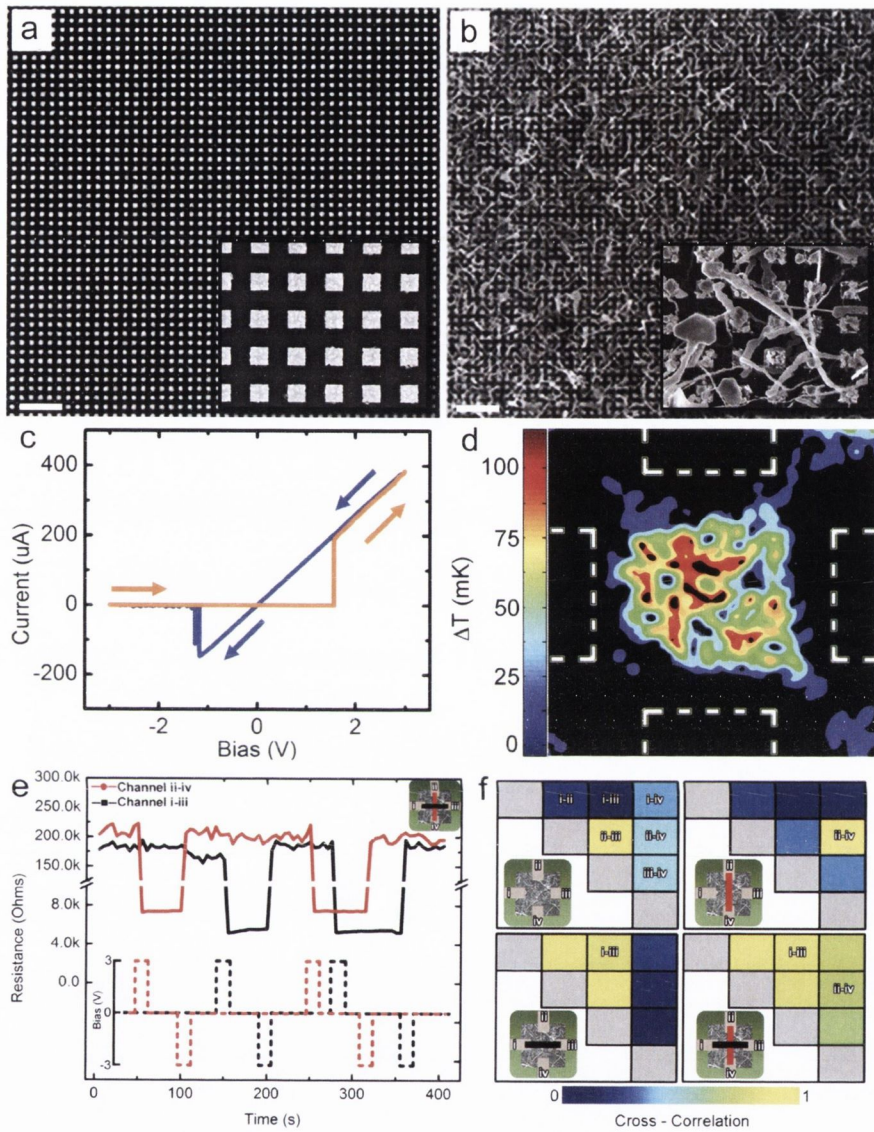
FIGURE 1.15. Neuromorphic networks of Ag/Ag_2S nanowires. Dense arrays of Cu seeds (a) are used to produce complex, 3-D networks of Ag nanofilaments through electroless deposition (b). (c) Upon sulfurization, these networks demonstrate bipolar resistive switching indicating an electrochemical metallization mechanism as in atomic switches. (d) IR imaging of the networks during conduction showed a global, distributed conductance indicated by the heat signature resulting from Joule heating. Co-existence of multiple memory states was demonstrated through pulsing opposing electrode pairs and measuring the conductance ((e) and (f)). A heat map describes the degree of correlation between electrode pairs from no correlation (blue), to full correlation (yellow). Reproduced from Stieg, 2012, and Avizienis, 2012.[124,125]

stability, rising and falling despite a constant bias. By analysing the temporal correlation of the discrete conductance states, it was shown that these networks demonstrate behaviour similar to that of spatiotemporal states associated with neural networks.[124]

In a follow up study, Avizienis et al. demonstrate what they call "weak" and "strong" memristance exhibited by these Ag/Ag_2S networks.[125] Prior to an electroforming step and the formation of the LRS, sweeping a voltage across the networks was shown to produce hysteretic I-V curves. This behaviour – termed weak memristance – was attributed to the reduction of Ag^+ ions and the gradual formation of conductive filaments in the junctions. At a certain voltage, the networks showed a large jump in conductance, indicating the complete formation of a low resistance conduction path through the network – termed hard memristance. Finally, these networks were shown to demonstrate interesting cross-correlation behaviour by switching the resistance states of adjacent networks. Shown in Figure 1.15(e) and (f), four electrodes contact a network in a perpendicular geometry. Opposing electrodes were then addressed and bipolar switching was demonstrated. Interestingly however, by switching the state of electrodes i–iii, the state of electrodes ii–iv remained unaffected, and vice versa. This behaviour was plotted for all electrode pairs as a heat map of no correlation (blue) to total correlation (yellow) (Figure 1.15(f)). This fascinating, and unexpected result illustrates the potential that the study of networks holds, particularly for introducing diverse, controllable behaviour into random systems.

These results highlight some very interesting features regarding the behaviour of random networks, and as such provide an extremely relevant comparison to the systems that are investigated in this thesis. By incorporating resistive switching functionality into the network, a resistive switching response was demonstrated that was attributed to a global contribution from all junctions in the network. IR imaging was used to demonstrate global distributed conduction, however the resistive switching could not be visualised. As part of this thesis, techniques are developed to visualise both the conduction paths in the absence of current, and also allow the visualisation of the resistive switching centres within complex networks. Ultimately the work by Stieg and Avizienis et al. helps to illustrate one of the central ideas of this thesis, that the incorporation of a non-linear element into an otherwise simple, random metallic system has a significant effect on the properties of that system, and that this can lead to new levels of functionality and new, technologically relevant materials.

1.6 THESIS OUTLINE

This thesis aims to describe the electrical behaviour of random networks of nanowires with resistive junctions. To this end, this chapter has discussed the motivation for this work, providing a detailed review of recent literature on the fields of nanowire networks, and resistive switching, as well as recent work on networks incorporating resistive switching junctions. Chapter 2 details the theory behind the many pieces of equipment used throughout this thesis, and discusses in detail the experimental methods used throughout. In chapter 3, the junction resistance of individual Ag and Ni nanowires are investigated, and results regarding

the impedance spectroscopic analysis of single junctions are presented. Chapter 4 examines the electrical activation and subsequent electrical stressing of polymer-coated Ag nanowire networks. The scaling behaviour of network activation through junction breakdown is investigated, and a model is introduced to describe the behaviour observed. In chapter 5, the behaviour of Ni/NiO core-shell nanowire networks is studied, and the emergent behaviour that results from the incorporation of resistive switching elements at the junctions is examined.

References

[1] FEYNMAN, R. P., *Engineering and Science* **1960**, *23*, 22–36.

[2] NOVOSELOV, K. S., GEIM, A. K., MOROZOV, S. V. ET AL., *Science* **2004**, *306*, 666–669.

[3] COLEMAN, J. N., LOTYA, M., O'NEILL, A. ET AL., *Science* **2011**, *331*, 568–571.

[4] IIJIMA, S. ET AL., *nature* **1991**, *354*, 56–58.

[5] MORALES, A. M. and LIEBER, C. M., *Science* **1998**, *279*, 208–211.

[6] WILEY, B., SUN, Y., MAYERS, B. ET AL., *Chemistry-A European Journal* **2005**, *11*, 454–463.

[7] ROUTKEVITCH, D., TAGER, A. A., HARUYAMA, J. ET AL., *IEEE Transactions on Electron Devices* **1996**, *43*, 1646–1658.

[8] PATOLSKY, F. and LIEBER, C. M., *Materials today* **2005**, *8*, 20–28.

[9] DATTOLI, E. N., WAN, Q., GUO, W. ET AL., *Nano Letters* **2007**, *7*, 2463–2469.

[10] WAN, Q., LI, Q., CHEN, Y. ET AL., *Applied Physics Letters* **2004**, *84*, 3654–3656.

[11] LI, Q., KOO, S.-M., RICHTER, C. ET AL., *Nanotechnology, IEEE Transactions on* **2007**, *6*, 256 –262.

[12] LI, Q., KOO, S.-M., EDELSTEIN, M. D. ET AL., *Nanotechnology* **2007**, *18*, 315202.

[13] DE, S., HIGGINS, T. M., LYONS, P. E. ET AL., *ACS Nano* **2009**, *3*, 1767–1774.

[14] MARKETWATCH.COM, *Flexible electronics market by components, and by geography - analysis and forecast to 2014 - 2020*, http://on.mktw.net/1oKvKTD, **2014**.

[15] HUANG, Y., DUAN, X., WEI, Q. ET AL., *Science* **2001**, *291*, 630–633.

[16] LIPOMI, D. J., VOSGUERITCHIAN, M., TEE, B. C. K. ET AL., *Nature Nanotechnology* **2011**, *6*, 788–792.

[17] TAKEI, K., TAKAHASHI, T., HO, J. C. ET AL., *Nature Materials* **2010**, *9*, 821–826.

[18] WEIZMANN, Y., CHENOWETH, D. M., and SWAGER, T. M., *Journal of the American Chemical Society* **2011**, *133*, 3238–3241.

[19] SERRE, P., TERNON, C., STAMBOULI, V. ET AL., *Sensors and Actuators B: Chemical* **2013**, *182*, 390 – 395.

[20] *Thomson Reuters – Web of Science*, http://apps.webofknowledge.com/.

[21] KUMAR, A. and ZHOU, C., *ACS nano* **2010**, *4*, 11–14.

[22] CHEN, Z., COTTERELL, B., WANG, W. ET AL., *Thin Solid Films* **2001**, *394*, 201–205.

[23] HECHT, D. S., HU, L., and IRVIN, G., *Advanced Materials* **2011**, *23*, 1482–1513.

[24] LANGLEY, D., GIUSTI, G., MAYOUSSE, C. ET AL., *Nanotechnology* **2013**, *24*, 452001.

[25] DE, S. and COLEMAN, J. N., *Mrs Bulletin* **2011**, *36*, 774–781.

[26] HU, L. B., KIM, H. S., LEE, J. Y. ET AL., *ACS Nano* **2010**, *4*, 2955–2963.

[27] MADARIA, A. R., KUMAR, A., ISHIKAWA, F. N. ET AL., *Nano Research* **2010**, *3*, 564–573.

[28] GARNETT, E. C., CAI, W., CHA, J. J. ET AL., *Nature Materials* **2012**, *11*, 241–249.

[29] VAN DE GROEP, J., SPINELLI, P., and POLMAN, A., *Nano letters* **2012**, *12*, 3138–3144.

[30] LEE, M.-S., LEE, K., KIM, S.-Y. ET AL., *Nano Letters* **2013**, *13*, 2814–2821.

[31] LEE, J., LEE, I., KIM, T.-S. ET AL., *Small* **2013**, *9*, 2887–2894.

[32] *Cambrios Technologies Corp.*, http://www.cambrios.com/products, **2014**.

[33] LEE, P., LEE, J., LEE, H. ET AL., *Advanced Materials* **2012**, *24*, 3326–3332.

[34] SOREL, S., LYONS, P. E., DE, S. ET AL., *Nanotechnology* **2012**, *23*, 185201.

[35] GAO, Y., JIANG, P., LIU, D. ET AL., *The Journal of Physical Chemistry B* **2004**, *108*, 12877–12881.

[36] LEE, J.-Y., CONNOR, S. T., CUI, Y. ET AL., *Nano Letters* **2008**, *8*, 689–692.

[37] SCARDACI, V., COULL, R., LYONS, P. E. ET AL., *Small* **2011**, *7*, 2621–2628.

[38] LANGLEY, D. P., LAGRANGE, M., GIUSTI, G. ET AL., *Nanoscale* **2014**.

[39] TOKUNO, T., NOGI, M., KARAKAWA, M. ET AL., *Nano Research* **2011**, *4*, 1215–1222.

[40] ZHU, S., GAO, Y., HU, B. ET AL., *Nanotechnology* **2013**, *24*, 335202.

[41] SONG, T.-B., CHEN, Y., CHUNG, C.-H. ET AL., *ACS Nano* **2014**, *8*, 2804–2811.

[42] MUTISO, R. M., SHERROTT, M. C., RATHMELL, A. R. ET AL., *ACS nano* **2013**, *7*, 7654–7663.

[43] WU, H., HU, L., ROWELL, M. W. ET AL., *Nano letters* **2010**, *10*, 4242–4248.

[44] RATHMELL, A. R. and WILEY, B. J., *Advanced Materials* **2011**, *23*, 4798–4803.

[45] RATHMELL, A. R., NGUYEN, M., CHI, M. F. ET AL., *Nano Letters* **2012**, *12*, 3193–3199.

[46] LYONS, P. E., DE, S., ELIAS, J. ET AL., *The Journal of Physical Chemistry Letters* **2011**, *2*, 3058–3062.

[47] SANCHEZ-IGLESIAS, A., RIVAS-MURIAS, B., GRZELCZAK, M. ET AL., *Nano Letters* **2012**, *12*, 6066–6070.

[48] MORAG, A., EZERSKY, V., FROUMIN, N. ET AL., *Chemical Communications* **2013**, *49*, 8552–8554.

[49] CHEN, Z., YE, S., STEWART, I. E. ET AL., *ACS nano* **2014**.

[50] SHARMA, A. K., *Advanced semiconductor memories: architectures, designs, and applications*, Wiley-IEEE Press, **2009**.

[51] ITRS, The international technology roadmap for semiconductors, Technical report, http://www.itrs.net/, **2013**.

[52] TEHRANI, S., CHEN, E., DURLAM, M. ET AL., in *Proceeding International Electron Devices Meeting*, pages 8–11.

[53] ÅKERMAN, J., *Science* **2005**, *308*, 508–510.

[54] FUJISAKI, Y., *Japanese Journal of Applied Physics* **2010**, *49*, 100001.

[55] RAOUX, S., BURR, G. W., BREITWISCH, M. J. ET AL., *IBM Journal of Research and Development* **2008**, *52*, 465–479.

[56] PIRAMANAYAGAM, S. and CHONG, T. C., *Developments in data storage: materials perspective*, John Wiley & Sons, **2011**.

[57] ENGEL, B., AKERMAN, J., BUTCHER, B. ET AL., *Magnetics, IEEE Transactions on* **2005**, *41*, 132–136.

[58] WASER, R. and AONO, M., *Nature Materials* **2007**, *6*, 833–840.

[59] HICKMOTT, T. W., *Journal of Applied Physics* **1962**, *33*, 2669–&.

[60] OVSHINSKY, S. R., *Phys. Rev. Lett.* **1968**, *21*, 1450–1453.

[61] BECK, A., BEDNORZ, J., GERBER, C. ET AL., *Applied Physics Letters* **2000**, *77*, 139–141.

[62] MA, L., PYO, S., OUYANG, J. ET AL., *Applied Physics Letters* **2003**, *82*, 1419–1421.

[63] SEO, S., LEE, M. J., SEO, D. H. ET AL., *Applied Physics Letters* **2004**, *85*, 5655–5657.

[64] SHIMA, H., TAKANO, F., AKINAGA, H. ET AL., *Applied physics letters* **2007**, *91*, 012901–012901.

[65] SCOTT, J. C. and BOZANO, L. D., *Advanced Materials* **2007**, *19*, 1452–1463.

[66] YAO, J., SUN, Z., ZHONG, L. ET AL., *Nano Letters* **2010**, *10*, 4105–4110.

[67] VALOV, I., WASER, R., JAMESON, J. R. ET AL., *Nanotechnology* **2011**, *22*, 254003.

[68] HIROSE, Y. and HIROSE, H., *Journal of Applied Physics* **1976**, *47*, 2767–2772.

[69] BRUCHHAUS, R., HONAL, M., SYMANCZYK, R. ET AL., *Journal of The Electrochemical Society* **2009**, *156*, H729–H733.

[70] KUND, M., BEITEL, G., PINNOW, C.-U. ET AL., in *Electron Devices Meeting, 2005. IEDM Technical Digest. IEEE International*, IEEE, pages 754–757.

[71] KIM, S.-W. and NISHI, Y., in *Non-Volatile Memory Technology Symposium, 2007. NVMTS'07*, IEEE, pages 76–78.

[72] TERABE, K., HASEGAWA, T., NAKAYAMA, T. ET AL., *Nature* **2005**, *433*, 47–50.

[73] GUO, X., SCHINDLER, C., MENZEL, S. ET AL., *Applied Physics Letters* **2007**, *91*, 133513.

[74] ARATANI, K., OHBA, K., MIZUGUCHI, T. ET AL., in *Electron Devices Meeting, 2007. IEDM 2007. IEEE International*, IEEE, pages 783–786.

[75] JEONG, D. S., SCHROEDER, H., and WASER, R., *Electrochemical and solid-state letters* **2007**, *10*, G51–G53.

[76] OKA, K., YANAGIDA, T., NAGASHIMA, K. ET AL., *Journal of the American Chemical Society* **2009**, *131*, 3434–3435.

[77] GOUX, L., CHEN, Y.-Y., PANTISANO, L. ET AL., *Electrochemical and Solid-State Letters* **2010**, *13*, G54–G56.

[78] ARGALL, F., *Solid-State Electronics* **1968**, *11*, 535–541.

[79] CHOI, B. J., JEONG, D. S., KIM, S. K. ET AL., *Journal of Applied Physics* **2005**, *98*, 033715–.

[80] YANG, J. J., ZHANG, M., STRACHAN, J. P. ET AL., *Applied Physics Letters* **2010**, *97*, 232102.

[81] LEE, H., CHEN, P., WU, T. ET AL., in *Electron Devices Meeting, 2008. IEDM 2008. IEEE International*, IEEE, pages 1–4.

[82] KIM, W., PARK, S. I., ZHANG, Z. ET AL., in *VLSI Technology (VLSIT), 2011 Symposium on*, IEEE, pages 22–23.

[83] CHIEN, W., CHEN, Y., CHEN, Y. ET AL., in *Electron Devices Meeting (IEDM), 2010 IEEE International*, IEEE, pages 19–2.

[84] MENZEL, S., WATERS, M., MARCHEWKA, A. ET AL., *Advanced Functional Materials* **2011**, *21*, 4487–4492.

[85] YANG, J. J., PICKETT, M. D., LI, X. M. ET AL., *Nature Nanotechnology* **2008**, *3*, 429–433.

[86] KAWAHARA, A., AZUMA, R., IKEDA, Y. ET AL., in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2012 IEEE International*, pages 432–434.

[87] YI LIU, T., YAN, T. H., SCHEUERLEIN, R. ET AL., in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2013 IEEE International*, pages 210–211.

[88] YANG, J. J., MIAO, F., PICKETT, M. D. ET AL., *Nanotechnology* **2009**, *20*, 215201.

[89] KIM, K. M., JEONG, D. S., and HWANG, C. S., *Nanotechnology* **2011**, *22*, 254002.

[90] CHEN, A., HADDAD, S., WU, Y.-C. ET AL., in *Electron Devices Meeting, 2005. IEDM Technical Digest. IEEE International*, IEEE, pages 746–749.

[91] GOVOREANU, B., KAR, G., CHEN, Y. ET AL., in *Electron Devices Meeting (IEDM), 2011 IEEE International*, IEEE, pages 31–6.

[92] ZHANG, Z., WU, Y., WONG, H.-P. ET AL., *Electron Device Letters, IEEE* **2013**, *34*, 1005–1007.

[93] TSAI, C.-L., XIONG, F., POP, E. ET AL., *ACS nano* **2013**, *7*, 5360–5366.

[94] PRALL, K., RAMASWAMY, N., KINNEY, W. ET AL., in *Memory Workshop (IMW), 2012 4th IEEE International*, IEEE, pages 1–5.

[95] GIBBONS, J. and BEADLE, W., *Solid-State Electronics* **1964**, *7*, 785 – 790.

[96] SHEN, W. C., MEI, C. Y., CHIH, Y.-D. ET AL., in *Electron Devices Meeting (IEDM), 2012 IEEE International*, IEEE, pages 31–6.

[97] CHANG, M.-F., WU, C.-W., KUO, C.-C. ET AL., in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2012 IEEE International*, IEEE, pages 434–436.

[98] JUNG, K., SEO, H., KIM, Y. ET AL., *Applied Physics Letters* **2007**, *90*, 052104.

[99] PARK, G.-S., LI, X.-S., KIM, D.-C. ET AL., *Applied Physics Letters* **2007**, *91*, 222103–222103.

[100] LEE, M.-J., HAN, S., JEON, S. H. ET AL., *Nano Letters* **2009**, *9*, 1476–1481.

[101] CHANG, S. H., LEE, J. S., CHAE, S. C. ET AL., *Physical Review Letters* **2009**, *102*, 026801.

[102] KWON, D.-H., KIM, K. M., JANG, J. H. ET AL., *Nature nanotechnology* **2010**, *5*, 148–153.

[103] ROHDE, C., CHOI, B. J., JEONG, D. S. ET AL., *Applied Physics Letters* **2005**, *86*, 262907–262907.

[104] IELMINI, D., NARDI, F., and CAGLI, C., *Electron Devices, IEEE Transactions on* **2011**, *58*, 3246–3253.

[105] RUSSO, U., IELMINI, D., CAGLI, C. ET AL., *Electron Devices, IEEE Transactions on* **2009**, *56*, 193–200.

[106] CHEN, Y., KANG, J., CHEN, B. ET AL., *Journal of Physics D: Applied Physics* **2012**, *45*, 065303.

[107] LEE, S., CHAE, S., CHANG, S. ET AL., *Applied Physics Letters* **2008**, *93*, 212105.

[108] TSUNODA, K., KINOSHITA, K., NOSHIRO, H. ET AL., in *Electron Devices Meeting, 2007. IEDM 2007. IEEE International*, IEEE, pages 767–770.

[109] TSENG, Y. H., SHEN, W. C., HUANG, C.-E. ET AL., in *Electron Devices Meeting (IEDM), 2010 IEEE International*, IEEE, pages 28–5.

[110] CHIEN, W.-C., LEE, M.-H., LEE, F.-M. ET AL., in *VLSI Technology (VLSIT), 2013 Symposium on*, IEEE, pages T100–T101.

[111] GOUX, L., LISONI, J., JURCZAK, M. ET AL., *Journal of Applied Physics* **2010**, *107*, 024512.

[112] IELMINI, D., CAGLI, C., NARDI, F. ET AL., *Journal of Physics D: Applied Physics* **2013**, *46*, 074006.

[113] KIM, S. I., LEE, J. H., CHANG, Y. W. ET AL., *Applied Physics Letters* **2008**, *93*.

[114] HERDERICK, E. D., REDDY, K. M., SAMPLE, R. N. ET AL., *Applied Physics Letters* **2009**, *95*. Herderick, Edward D. Reddy, Kongara M. Sample, Rachel N. Draskovic, Thomas I. Padture, Nitin P.

[115] OKA, K., YANAGIDA, T., NAGASHIMA, K. ET AL., *Journal of the American Chemical Society* **2010**, *132*, 6634–+.

[116] TRESBACK, J. S., VASILIEV, A. L., PADTURE, N. P. ET AL., *IEEE Transactions on Nanotechnology* **2007**, *6*, 676.

[117] BRIVIO, S., TALLARIDA, G., PEREGO, D. ET AL., *Applied Physics Letters* **2012**, *101*, 223510.

[118] DONG, Y., YU, G., MCALPINE, M. C. ET AL., *Nano Letters* **2008**, *8*, 386–391.

[119] HE, L., LIAO, Z.-M., WU, H.-C. ET AL., *Nano Letters* **2011**, *11*, 4601–4606.

[120] CHA, E., WOO, J., LEE, D. ET AL., in *Circuits and Systems (ISCAS), 2014 IEEE International Symposium on*, IEEE, pages 428–431.

[121] CAGLI, C., NARDI, F., HARTENECK, B. ET AL., *Small* **2011**, *7*, 2899–2905.

[122] WHANG, D., JIN, S., WU, Y. ET AL., *Nano Letters* **2003**, *3*, 1255–1259.

[123] INCE, D. C., editor, *Mechanical Intelligence: Collected Works of A.M. Turing*, North-Holland Publishing Co., **1992**.

[124] STIEG, A. Z., AVIZIENIS, A. V., SILLIN, H. O. ET AL., *Advanced Materials* **2012**, *24*, 286–293.

[125] AVIZIENIS, A. V., SILLIN, H. O., MARTIN-OLMOS, C. ET AL., *PloS one* **2012**, *7*, e42772.

2

EQUIPMENT & METHODS

A wide variety of equipment, techniques, and methods are used throughout this thesis to fabricate, image, analyse, and measure samples. This chapter focuses on describing each of these methods in detail, as well as discussing the various pieces of equipment and the theory behind their operation. Sample fabrication methods are described in full, as are the electrical characterisation methods used.

2.1 MICROSCOPY

The microscope, whether optical, electron, or force, is a ubiquitous tool in the field of nanoscience. It routinely enables users to view objects on the nanoscale, and the most sophisticated systems can observe individual atoms. Multiple advanced microscope systems were used in this work, for both analysis and fabrication. The operation and theory behind each are described in this section.

2.1.1 SCANNING ELECTRON MICROSCOPY

The electron microscope is an enormously powerful tool, capable of high resolution imaging (transmission electron microscopy (TEM), and scanning electron microscopy (SEM)), quantitative material analysis (energy dispersive x-ray spectroscopy (EDX)), as well as nanofabrication (electron beam lithography (EBL)). This work utilises all of these capabilities using a suite of microscopes provided by the Advanced Microscopy Laboratory, including the Zeiss Supra 40 scanning electron microscope, the Zeiss Ultra Plus scanning electron microscope, and the FEI Titan transmission electron microscope.

The first electron microscope developed was a transmission electron microscope, in 1931.[1] Its invention built on the work of Louis de Broglie, who in 1924 showed that an electron could act as a wave, with an associated wavelength (de Broglie wavelength) given by $\lambda = h/mv$, where h is Planck's constant, and m and v are the mass and velocity of the
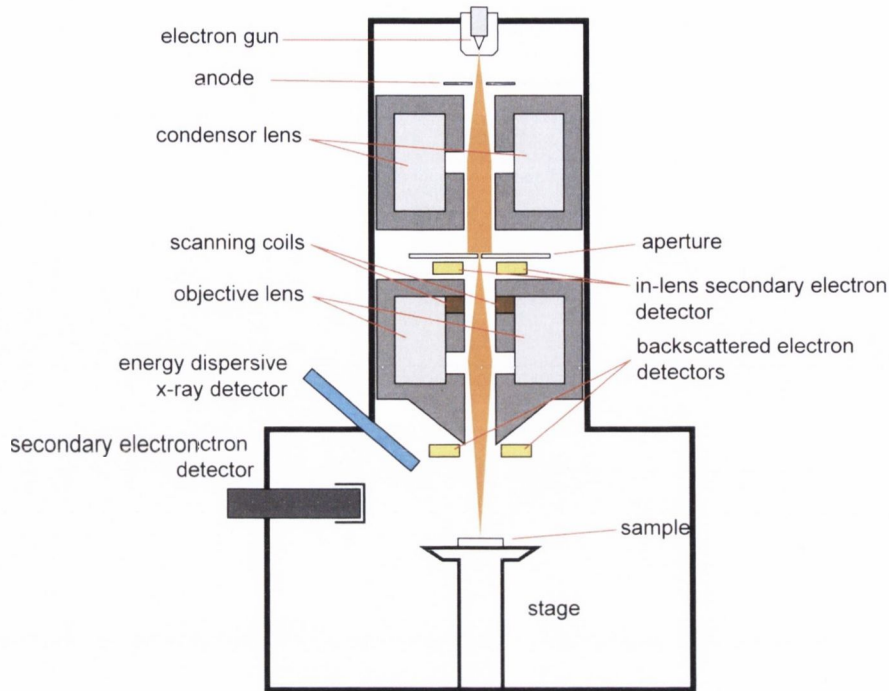
FIGURE 2.1. Schematic illustration of a scanning electron microscope.

electron respectively. In 1873, the German optician Ernst Abbe observed that the diffraction-limited resolving power of a conventional microscope was $d = 0.61\lambda/n.sin\theta$, where n is the refractive index of the medium and θ is the half-angle subtended by the lens at the object. For white light, this corresponds to ~ 300 nm. Using de Broglie's relationship, an electron accelerated through 100 kV has a de Broglie wavelength of 0.0037 nm, or a theoretical resolution of ~ 1.6 pm. Due to lens imperfections and sample interactions however, these limits are rarely ever achieved, though modern TEMs are routinely capable of achieving sub-nanometre resolutions.

A schematic of a modern SEM is shown in Figure 2.1. The basic operation is very similar to that of a conventional light microscope. High voltage (0.5 – 30 kV) accelerates a beam of electrons away from a source. Condenser and objective magnetic lenses focus the electron beam onto the sample, while the variable aperture limits beam width, and scanning coils raster the beam across the surface. Multiple detectors may be housed within the microscope to collect the various forms of electrons produced by the electron/sample interaction (see Figure 2.2). High energy electrons incident upon a surface interact with atoms within the sample via elastic and inelastic collisions. Inelastic collisions can result in outer shell electrons becoming dislodged from sample atoms, producing *secondary electrons* (SE). Low energy (< 50 eV) electrons such as these will only be emitted to the vacuum if they are within an escape distance, R, of the surface, and thus possess information about the surface. Incident electrons may also undergo many elastic collisions, causing them to deviate from their original path, and finally emerge from the surface as *backscattered electrons* (BSE). Depending on the number of collisions, their energy can vary significantly,
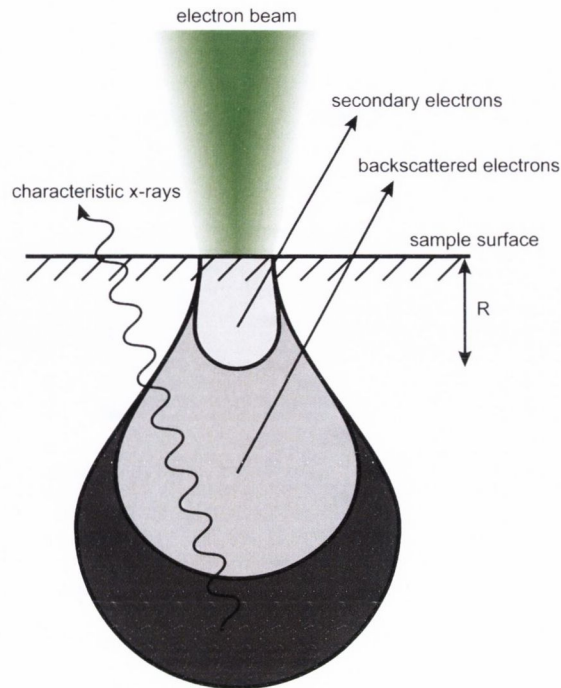
FIGURE 2.2. Electron beam – surface interaction. High energy electrons incident upon a surface interact with that surface in a number of different ways. Inelastic collision produces low energy, secondary electrons. Only those secondary electrons produced within the escape distance, R, are emitted from the surface. Backscattered electrons are those that have been deflected through elastic collisions such that they emerge from the surface once again. Characteristic x-rays are produced by the recombination of an electron and a hole created by the inelastic collision of an incident electron with an core electron.

and the yield of BSEs has a steep dependence on the atomic number of the scattering atoms. As a result, when detected, variations in atomic number then will produce regions of varying intensity in an SEM image, enabling differences in elemental composition to be distinguished. Characteristic x-rays are also produced as a result of interactions with the incident electron beam. This is expanded upon in section 2.1.1.2.

Electron microscopes may use one of three types of electron source: tungsten, lanthanum hexaboride (LaB_6), and a field emission gun (FEG). Both W and LaB_6 sources operate on the principle of thermionic emission. The filament is heated such that spontaneous electron emission occurs. A high voltage between the source and an anode accelerates the electrons and produces the beam. LaB_6 has a lower work function than W, and is the preferred choice due to higher efficiency. Field emission guns operate on a much different principle. By fabricating a W needle with a very sharp tip (radius $< 1\,\mu$m), extremely high electric fields can be generated at the apex. The high field ($\sim 10^{10}\,V\,m^{-1}$) narrows the surface energy barrier to such an extent that electrons may tunnel across it, even at room temperature – this is known as cold field emission (CFE).

The important characteristics of the electron source are the brightness ($A\,cm^{-2}\,sr$) and size. Due to the extremely sharp tip of a FEG, the brightness is three orders of magnitude

TABLE 2.1. Comparison of electron sources.[2]

	Tungsten	LaB_6	CFE FEG	SE FEG
Brightness (A cm^{-2} sr)	10^6	10^6	10^9	10^8
Size	20–50 μm	10–20 μm	5–10 nm	15 nm
Vacuum requirement (mbar)	$<10^{-4}$	$<10^{-6}$	$<10^{-10}$	$<10^{-8}$
Operating temp. (K)	2800	1400–2000	300	1800
Lifetime (h)	100	600	>1000	>2000

higher than either W or LaB_6 guns. Unfortunately however, due to the sensitivity of the cathode to surface adsorbents, cold FEGs require much higher operational vacuums as well as regular flashes to remove adsorbents. An alternative to the CFE is the Schottky emitter (SE) FEG. A monatomic layer of ZrO is formed on a flattened tungsten (100) tip, lowering the work function from 4.54 eV to 2.8 eV,[2] and thereby reducing the barrier to tunnelling. Operated at 1800 K, the SE FEG is not as bright as a CFE, but produces stable currents and its operation is also less demanding, resulting in less downtime. All SEMs used in this work use a SE FEG source. The characteristics of each type of electron source are tabulated in table 2.1.

2.1.1.1 Imaging & Contrast in SEM

A secondary electron SEM image of Au and Ni on SiO_2 is shown in Figure 2.3(a), taken using a standard Everhart-Thornley SE detector,[3] and known in this work as the SE2 detector. Figure 2.3(b) shows a high magnification image of a Ni electrode contacting a nanowire on SiO_2, taken using an In-lens detector. As the name suggests, the In-lens is housed within the electron column, while the SE2 detector is housed outside the column (see Figure 2.1). The primary advantage of the SE2 detector is the contrast generated between different materials, particularly when the difference in atomic number is large. In the example shown, contrast is visible between all three materials shown: Au, Ni, and SiO_2, with the materials of higher atomic number appearing brighter. The In-lens detector is not as sensitive to variations in material, however its surface sensitivity is much higher than that of the SE2. The example in Figure 2.3(b) shows large amounts of surface detail, making it ideal for high magnification imaging. The difference in contrast and topographic sensitivity is primarily due to different secondary electrons reaching the detector. It is thought that lower energy secondary electrons, generated from the primary incident beam (type-I), as well as high energy backscattered secondary electrons (type-II) make up the In-lens image, while only higher energy type-II electrons make up the SE2 image.[4] As backscattered electron intensity depends strongly on atomic number,[2] SE2 material contrast should then show a similar relationship. Figure 2.3(a) demonstrates this to be the case, as the higher
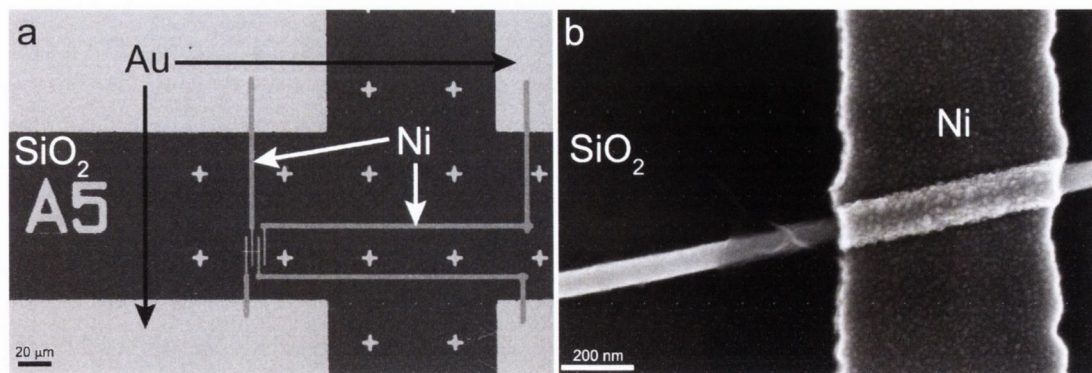
FIGURE 2.3. Secondary electron imaging in SEM. (a) Secondary electron image of Au and Ni electrodes on a SiO_2 substrate using the SE2 detector. (b) High magnification secondary electron image of Ni electrode on SiO_2 taken using the In-lens detector. The greater sensitivity of the Inlens detector to surface detail makes it ideal for high magnification imaging such as this. Both images were taken at an accelerating voltage of 5 kV.

atomic number materials (Ni and Au) appear brighter.

In the semiconductor industry, having a fast method to determine the location of shorts (or opens) in a device or chip is of great importance. To this end, *passive voltage contrast* (PVC) SEM imaging was developed.[5] PVC uses the biasing created by the electron beam to generate contrast in the secondary electron image, and in that way may be used to locate floating objects relative to a grounded environment. Figure 2.4 shows the secondary electron yield plotted against primary beam energy. A small range of beam energies exist (typically 1-2 keV) where the SE yield (δ) is greater than unity, that is, more electrons are emitted as secondary electrons than are incident upon the surface.[6,7] When operated in this energy range, a net positive charge builds up in the material. If the object is grounded, this positive charge may simply be drawn away. If not however, in an effort to maintain charge neutrality further secondary electron emission from the surface is impeded, creating a darkened region within the image.[6] In chapter 4, a variation on this contrast mechanism is used to visualise connectivity within a network of Ag nanowires.

2.1.1.2 Energy Dispersive X-ray Spectroscopy

A material bombarded with electrons produces x-rays of two kinds. The first kind, known as *Bremsstrahlung* radiation, is produced as electrons are deflected (accelerated) by charged particles within the material, creating a continuous distribution of wavelengths.[8] The second is a discrete set of wavelengths that form a characteristic spectrum for each element. Energy dispersive x-ray spectroscopy (EDX) uses these characteristic lines for elemental analysis.

High energy incident electrons knock out core electrons via an inelastic collision. The hole created by this event is filled by an electron in a higher energy shell, and the excess energy is released in the form of a photon of x-radiation. Figure 2.5(a) shows a schematic of
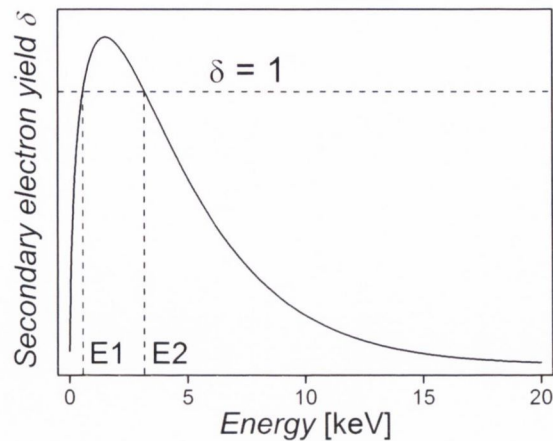
FIGURE 2.4. Secondary electron yield as a function of primary beam energy. Beam energy between E1 and E2 produces a greater number of secondary electrons than are incident via the primary beam. This produces a net positive charge, which if not grounded will impede the emission of further secondary electrons thereby producing a dark feature in the SEM image. [6,7]

this process. The nomenclature is such that the radiation produced as a K-shell hole is filled by an L-shell electron is termed the Kα line. The energy levels of each element will vary such that each EDX spectrum is unique. Figure 2.5(b) shows a spectrum for Pt on Al_2O_3 bombarded by 20 keV electrons, where x-ray intensity is plotted against x-ray energy. The characteristic lines available to be excited depend on the energy of the incident beam, as does their relative intensity. In the example shown in Figure 2.5(b), only lines up to 20 keV are available, and it can be seen that the intensity of the spectrum falls off approaching this value. For the most efficient x-ray production, the energy of the beam should be 3–4 times that of the line. There is also a soft cut off at low x-ray energy (below 1 keV), where the x-rays are absorbed before ever reaching the detector. [2]

Housed within the SEM chamber, an EDX detector consists of either Li-drifted silicon, or high-purity intrinsic germanium, which act as a diode under reverse bias. Incident x-rays generate photoelectrons in the semiconductor, reducing the barrier to electron flow. A current spike is then generated whose magnitude is proportional to the energy of the incident photon, and which is then fed into a multichannel analyser. The detector is then able to measure multiple energies simultaneously, reducing measurement time significantly. One limitation of EDX is the requirement of thick samples. As illustrated in Figure 2.2, characteristic x-rays are produced deep within the surface, and as the accelerating voltage is increased so too is the depth at which the x-rays are produced. Thus, for nanoscale thickness materials EDX may not provide quantitative analysis as substrate signals begin to dominate, and atomic ratios become unclear. The highest quality EDX analysis is performed within a TEM, as much higher accelerating voltages (up to 300 kV) are available, allowing much higher energy lines to be resolved. Additionally, quantitative elemental analysis of nanoscale objects may be performed, as the TEM grid produces no substrate signal.
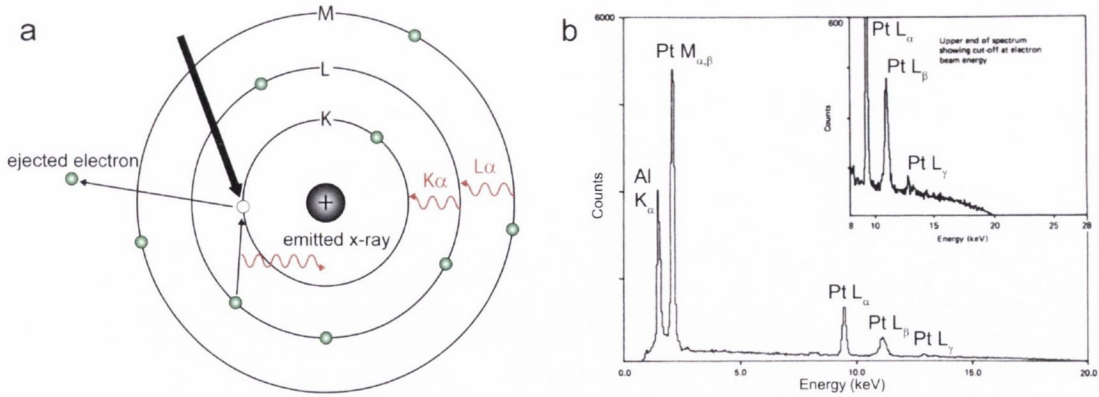
FIGURE 2.5. (a) Schematic showing the production of characteristic x-rays by electron bombardment, and (b) EDX spectrum of a Pt/Al_2O_3 sample. The characteristic lines of both Al and Pt are visible. Oxygen is not visible on this spectrum as its $K\alpha$ line is located at 0.525 keV, below the soft cut off. The inset shows the gradual fade off of the Bremsstrahlung background up to 20 keV. Adapted from Watt, 1997.[2]

2.1.2 ELECTRON BEAM LITHOGRAPHY

As mentioned in section 2.1.1, electron microscopes may be used not only as microscopes but also as nanofabrication tools through a technique called electron beam lithography (EBL). One of the first demonstrations of EBL was made by Mollenstedt and Speidel in 1961,[9] little over a year after Feynman's "There's plenty of room at the bottom" lecture. Fifteen years later the technology had progressed to the point that sub-10 nm lines could be fabricated.[10] Today EBL is regularly used in research to fabricate nanoscale features unachievable through optical lithographic methods. In recent years, the use of EBL has become economically viable for the semiconductor industry as the costs of continually improving optical lithographic methods escalates, though due to its serial nature it remains a very slow process in comparison.[11]

EBL operates on the same principles as standard optical lithography: a thin film of electron sensitive resist is spun onto the sample, baked to remove the solvent, and subsequently exposed to the electron beam (e-beam). The beam alters the resist in the exposed areas relative to the unexposed regions such that the pattern may be revealed by dissolution in a developer. EBL does not require a hard mask however, rather a focused e-beam is scanned across the surface in the pattern desired by the user. This allows for enormous flexibility in design, and also allows changes to be made as needed, from sample to sample. This process flow is illustrated in Figure 2.6. Proprietary software (Raith GmbH) is used to both fabricate the pattern and control the electron beam. Beam blanker plates must be installed in the SEM column for EBL operation. These direct the beam away from the sample at very high speeds, controlling the exposure.

Resists may be positive- or negative-tone. Positive-tone resists are altered by the e-beam such that they become soluble in the developer and the exposed areas are therefore removed, while negative-tone resists become less soluble upon exposure, and thus only the exposed
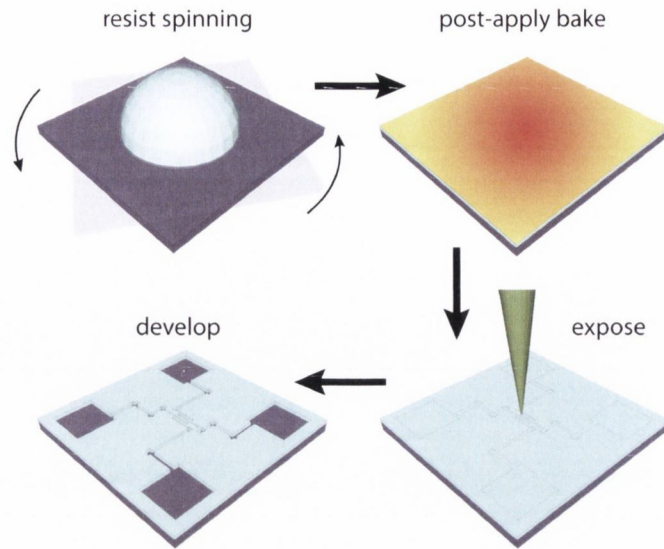
FIGURE 2.6. Electron beam lithography work flow.

areas remain once developed. Polymethyl-methacrylate (PMMA) is the most common positive resist used for EBL. Exposure to the beam induces two reactions: bond-breaking, and polymerization. For PMMA, bond breaking is most prevalent, due to the relatively weak carbon-carbon and carbon-hydrogen bonds,[11] which increases the solubility of the polymer in the developer. Hydrogen silsesquioxane (HSQ) is an example of a negative tone resist. Exposure to the beam induces polymerization via cross-linking of the polymer chains, thereby reducing its solubility.

Due to the multiple scattering events available to the incident electrons, choice of accelerating voltage is of critical importance to the resolution of the final pattern. Figure 2.7 illustrates this issue via Monte Carlo simulations of the electron beam incident upon a $PMMA/SiO_2/Si$ sample at a range of accelerating voltages. At low accelerating voltages the beam may not have enough energy to fully penetrate the resist (Figure 2.7(a)). Forward scattering of the incident electrons broadens the beam within the resist, increasing the line width and ultimately blurring the features.[12] Figure 2.7(b) shows an example of this. An accelerating voltage of 15 kV (Figure 2.7(c)) is appropriate as the beam broadening is not extensive, but enough to create an undercut in the resist, ideal for metal deposition. Backscattered electrons generated in the substrate however, can expose regions up to 100 nm away from the beam. This phenomenon, known as the proximity effect, limits the feature pitch as one exposure effectively increases the dose received by another, within a certain radius. The 100 kV beam shows almost no beam broadening or backscattered electrons, and is thus ideal for high resolution lithography. Most SEM-EBL systems however are not capable of supplying such high beam energies. Additionally, the clearing dose ($\mu C\,cm^{-2}$), that required to fully expose the resist, is proportional to the beam energy,[13] resulting in longer exposure times at higher beam energies.
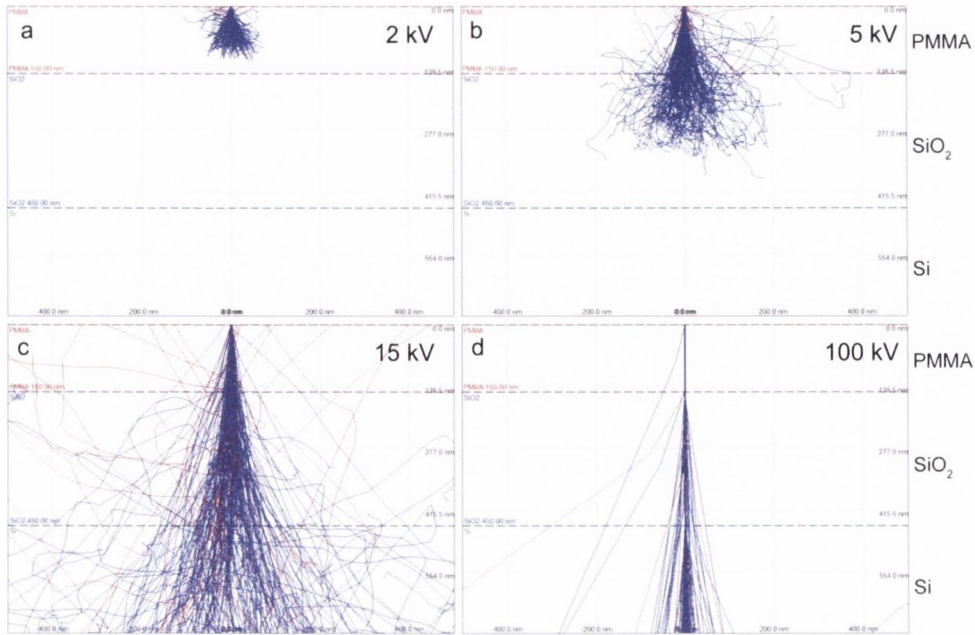
FIGURE 2.7. Monte Carlo simulations of electron/sample interactions for a range of accelerating voltages: (a) 2 kV; (b) 5 kV; (c) 15 kV; and (d) 100 kV. Substrate is a PMMA(150 nm)/SiO_2(300 nm)/Si stack. Simulations generated using CASINO software.[14,15] Blue lines represent primary electrons, while red lines represent backscattered electrons.

2.1.3 HELIUM ION MICROSCOPY

In 2006, researchers working at the Atomic Level Imaging Systems build the first commercially viable helium ion microscope (HIM).[16] Its birth was a long one, having its origins in the field ion microscope first demonstrated by Müller in 1956.[17] While only a small number of these instruments have been produced to date, the demonstrated capabilities make it an exciting technology for the future. In this work, the Zeiss Orion Plus Helium Ion Microscope, provided by the Advanced Microscopy Laboratory, was used.

The HIM works on many of the same principles as an SEM. A beam of charged particles is accelerated toward a surface, magnetic condenser and objective lenses collimate and focus the beam respectively, while scanning coils raster the beam across the sample. An Everhart-Thornley detector in the sample chamber detects secondary electrons produced via interactions of the primary beam with the surface, and creates an image. Rather than an electron source however, the HIM uses ionised He atoms produced via field ionisation from a single atomic point, creating an incredibly small beam size as schematically illustrated in Figure 2.8. A W tip is formed such that there is a single atom at the apex, which evaporates off under high fields, leaving behind three atoms at the tip, known as a *trimer*. The voltage on the tip is such that only at the trimer is the field strong enough to cause ionisation. The tip is then oriented is such a way that the ion beam from only one of the three atoms is directed to the sample, while the other beams are wasted on the anode. As the current is shared by only three atoms, the brightness of the source is very high: 4×10^9 A cm^{-2} sr for
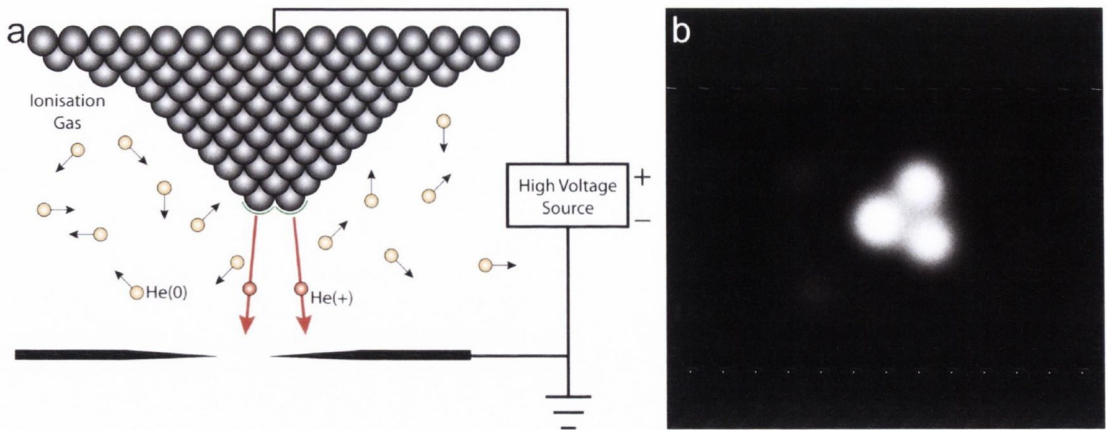
FIGURE 2.8. Helium ion beam generation. (a) Field ionization at a 3-atom point (trimer) produces beams of He^+ ions. The tip is oriented such that only one of the three atoms produces the primary imaging beam, while the other two are wasted upon the anode. (b) Field ion micrograph showing emission from trimer. Bright spots indicate high beam intensity. Reproduced from Economou, 2012.[19]

a 20 kV extraction voltage.[16,18]

To date the highest resolution achieved by a HIM is 0.35 nm,[19] three times better than even the most sophisticated SEM. Additionally, the convergence angle of the beam is five times smaller than that of an electron beam, which makes the depth of field correspondingly five times larger. This has significant advantages when imaging larger, 3-dimensional objects. The HIM is also much more sensitive to surface detail, due to a number of factors. The standard imaging mode in HIM, as in SEM, is via secondary electron detection. The SE yield due to helium ion interaction ranges from 3 to 10 depending on the material,[16] compared to ~ 1 for SEM (see Figure 2.4), and so SE images produced by a HIM demonstrate significantly lower noise levels. The helium ion interaction volume is also substantially smaller than that for electrons due to the larger mass of the ion, so the SE signal is not distorted by de-localised, type-II SEs. In addition to this, the ratio of type-I to type-II electron production is lower for He ions than for electrons,[20] resulting in an imaging mode that is far more sensitive to surface detail than its equivalent in SEM.

Secondary electron production is the result of the inelastic collision between He^+ ions and atoms within the sample, however another event may also occur resulting in scattering of the incident ions, known as Rutherford backscattering. High energy incident ions are repelled by Coulomb forces from the large, positively charged nuclei. These are then detected and an image formed in a technique known as Rutherford backscattered ion imaging (RBI).[18] The scattering yield shows a dependence on the atomic number of the species, and thus RBI may be used for material analysis by distinguishing elemental differences in a sample.[21]

The HIM presents some interesting opportunities, not simply confined to imaging. Just as an electron beam may be used to expose electron sensitive resists in EBL, HIM may be similarly used as a lithographic tool, and due to its sharper beam size and smaller interaction
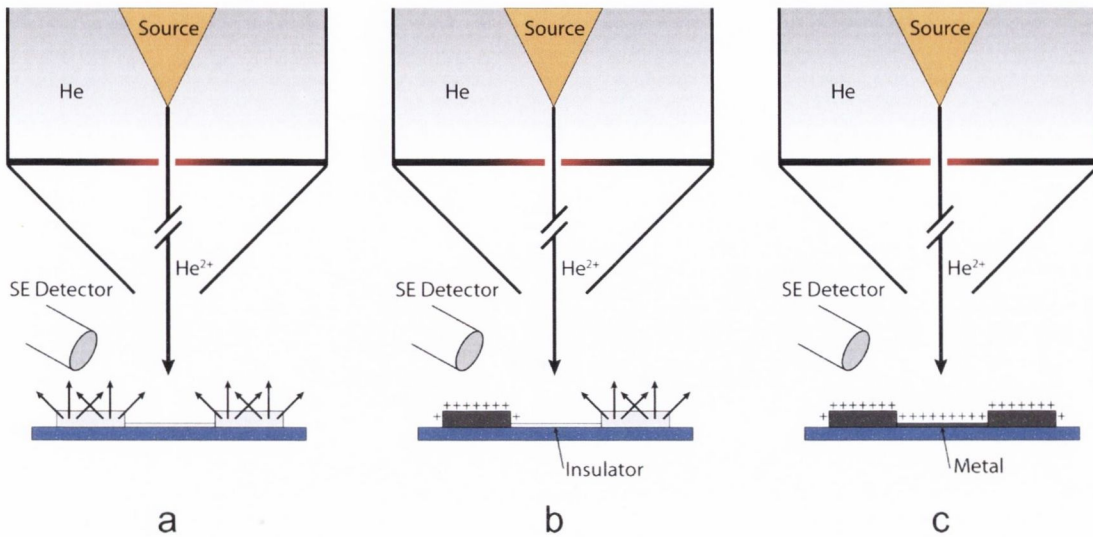
FIGURE 2.9. Passive voltage contrast technique in the HIM. (a) Secondary electrons are produced by interactions with the primary ion beam. (b) Dosing an object with He$^+$ ions causes large positive charge to build up, if not grounded. Secondary electron emission will be impeded by the charged surface, producing darkened features in the image. (c) Charge will dissipate to any objects that are metallically connected to the original dose point. In this way it is possible to map electrical connectivity between objects.

volume, already looks to surpass EBL as a nanofabrication tool.[22,23] The ion beam may also be used to etch or mill a surface as in focused ion beam (FIB) microscopy, though the He$^+$ ions are significantly less destructive than the Ga$^+$ beam used in FIB. As a result it is a far more effective tool to mill fine structures in materials such as graphene, which are extremely sensitive to edge effects and dopant contamination.[24]

2.1.3.1 Passive Voltage Contrast HIM

HIM may also be used to generate passive voltage contrast images, as in SEM. As mentioned in chapter 1, nanowire networks are of extreme technological value, from both a materials and device perspective. Studying the connectivity within networks is of central importance to advancement within this area, and is the main focus of this thesis. To this end, and as part of this work, a HIM-based passive voltage contrast technique has been developed that is capable of mapping the electrical connectivity within a random network of nanowires. The passive voltage contrast mechanism in HIM is largely similar to that in SEM. A positive surface charge impedes the escape of secondary electrons, generating contrast in the secondary electron image. Unlike SEM however, positive charge build up is due to both super-unity SE yield as well as He$^+$ implantation, generating a very strong contrast signal.

As will be discussed in section 2.3, a contacted nanowire network consists of metal pads (usually Ni) making contact to an underlying thin film network of nanowires. Adjacent pads are addressed electrically (section 2.4) to determine, and manipulate, the resistance of the network and the degree of connectivity within the network. A pre-determined amount
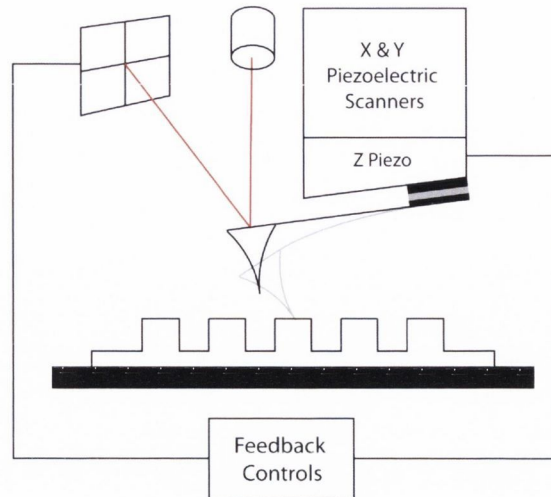
FIGURE 2.10. Diagram illustrating the basic components required for AFM operation. x- and y-piezoelectric scanners move the tip across a surface as another piezoelectric material oscillates the cantilever at its resonance frequency. A laser is reflected off the cantilever and onto a photodiode which detects changes in the oscillation amplitude, causing a feedback mechanism to move the tip in the z-axis such that the amplitude remains constant.

of charge is injected into one of these metal pads via the ion beam, in a process termed "dosing". In order that the charge is not neutralised by SE production, the beam is blanked, or directed away from the sample, immediately following the dosing step and prior to image acquisition. An SE image of the pad and connected network is then obtained. The charge dosing generates contrast in the SE image such that any object electrically connected to the dosed pad will show up dark as the charge diffuses to these areas. Figure 2.9 schematically illustrates this contrast mechanism. The degree of contrast seen in the final image then depends on a number of factors: *a*) the size of the pad and surrounding network; *b*) the amount of charge dosed; and *c*) the time taken to acquire the image – the longer the image acquisition time, the lower the noise, however a greater amount of charge will be neutralised through SE generation.

In chapter 5, this PVC technique is used to map the connectivity of Ni nanowire networks through various stages of activation, and will also be used to image a resistive switching network in both the LRS and HRS.

2.1.4 ATOMIC FORCE MICROSCOPY

Atomic force microscopy (AFM) is an incredibly powerful technique used for visualising various properties of a surface. Since its invention in 1986 by Binnig et al.,[25] the atomic force microscope has grown from a simplistic force detection probe to one of the most widely used and versatile microscope systems in modern research. Unlike conventional microscopes which *see* a surface by focusing a two dimensional projection of a surface onto a screen, the AFM *feels* the surface with a sharp probe, and in this way builds up a three dimensional map of the underlying features. This presents some immediate advantages: as
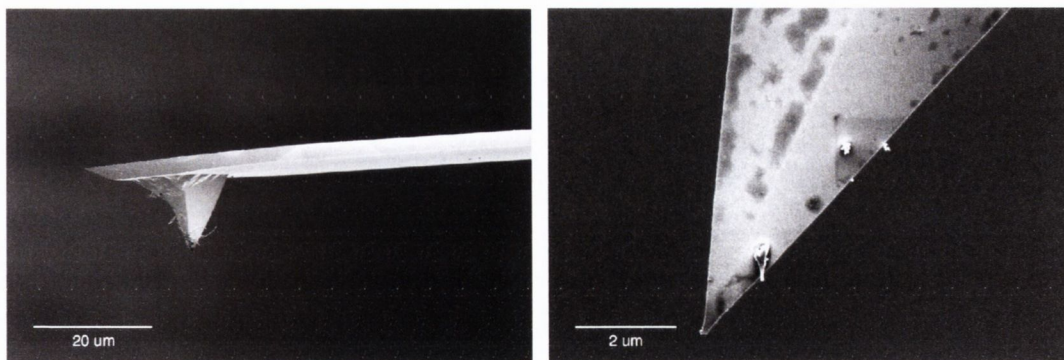
FIGURE 2.11. Atomic force microscopy tips. Tips are made from Si or SiN and are fabricated on the end of cantilevers. The tip diameter is typically 20 nm, although ultra sharp tips are available with diameters of ~ 2 nm. The length, width and the material from which it is made all determine the resonance frequency and force constant of each cantilever, which in turn affect the imaging capabilities. Tips may be received coated in various materials for specific purposes, e.g. electrical, magnetic, or biological applications.

the ultimate limit to the resolving power of the microscope is the sharpness of the tip, atomic resolution is not only possible, but has been achieved with remarkable results[26]. Secondly, neither the surface type nor the environment affect the measurement as significantly as in scanning tunnelling microscopy (STM). An insulating surface can therefore be imaged in ambient atmosphere, just as a conducting sample may be imaged in ultra high vacuum, or a biological sample in buffers at 37 °C. Although most AFM systems cannot operate at the same speeds or with the same freedom as an electron microscope*, the ability to operate in multiple environments and measure multiple properties of a surface makes AFM an invaluable tool in the field of nanoscience.

The AFM operates by scanning a sharp tip on the end of a cantilever across a surface in a raster pattern. The movement of the tip is measured with extremely high accuracy using an optical lever system (see Figure 2.10). A laser is reflected off the back of the cantilever and onto a photosensitive diode which detects the motion of the cantilever perpendicular to the surface. A typical optical lever can resolve movements on the order of picometers in the z-axis. Each pass of the AFM tip takes a 2-dimensional profile of the surface, completing a 3-dimensional image as the raster pattern builds. The ability to take high resolution topographical images is just one of many uses for the AFM. There are many modes in which the AFM can operate, each revealing a particular property of the underlying surface. Those used in this work are discussed below.

2.1.4.1 Static & Dynamic Mode AFM

The original and most basic mode available to the AFM user is contact mode, so-called because the tip is in constant contact with the sample. The interaction force lies in the

---

*Some specialised high-speed systems can now operate at video frame rates.[27]
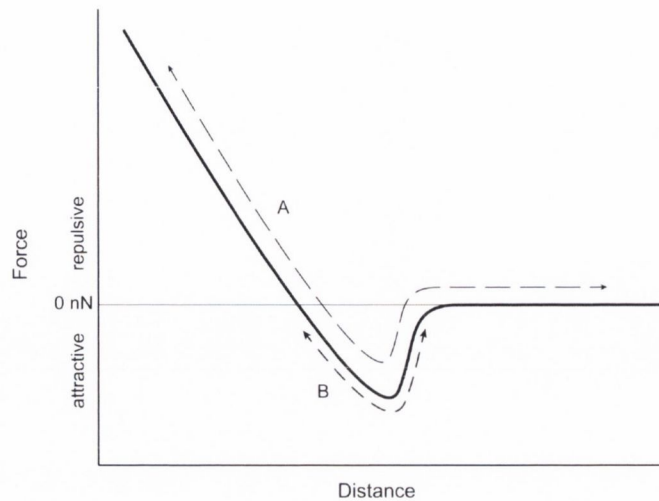
FIGURE 2.12. Force – Distance plot showing the interaction of an AFM tip with a surface. Two regions are shown, the repulsive region, A, and the attractive region B. The attractive region occurs at small distances as Van der Waals forces aim to bring the tip in contact with the surface such that the cantilever experiences negative forces. The repulsive region occurs due to short range repulsions as the tip makes contact with the surface. Modified from Eaton and West, 2010.[28]

repulsive regime of a force-distance plot, as in Figure 2.12. Contact mode can be thought analogous to a stylus moving over a record in a record player. To obtain a topographic image in contact mode, a constant force is maintained between the tip and the sample. This is achieved by maintaining a constant deflection of the optical lever through a feedback mechanism (Figure 2.10). As the underlying topography changes, the feedback loop drives a piezoelectric element to move the lever in the z-axis such that the deflection remains constant. As a result of the repulsive forces applied between tip and sample, both may be damaged during scanning. The forces applied to the sample can be estimated from Hooke's Law:

$$F = k \times D \tag{2.1}$$

where F is the force, k is the force constant of the tip, and D is the deflection distance of the tip. Each tip must be calibrated to determine its optical lever sensitivity before force measurements can be made. Contact mode may achieve much higher resolution than dynamic modes, particularly in liquid where capillary forces between tip and surface are not an issue.[28]

Initially, contact mode was the only mode available to the AFM user. Over the years however many different modes have been developed to suit different samples or to probe different properties of the sample. There are at least 20 different modes available to the modern AFM user,[28] with more in development. This perhaps demonstrates the versatility of the tool. Most of these stem from the ability to monitor changes to the amplitude, phase or frequency of an oscillating cantilever caused by interactions with the surface. These are so-called dynamic modes.

As mentioned above, one of the disadvantages of using contact mode AFM is the high forces associated with it, and the damage this can do the sample, the tip, or both. Dynamic, or tapping AFM modes work around this by oscillating the cantilever at or near it resonant frequency ($\sim$ tens of kHz) such that it spends very little, if any time in contact with the sample. By detecting changes in the amplitude of this oscillation through the optical lever, the feedback loop adjusts the height of the cantilever such that the amplitude remains constant. Two regimes exist in dynamic AFM, as depicted in Figure 2.12: (a) intermittent-contact mode; and (b) non-contact mode. Intermittent-contact and tapping modes are synonymous and operate by oscillating the cantilever at high amplitude, where changes in the amplitude are used to control the feedback loop. The tip travels between both attractive and repulsive regions as shown in Figure 2.12. Non-contact is slightly different as it operates by oscillating the cantilever away from resonance so the amplitudes are small and the tip remains in the attractive region of the force curve. Non-contact mode is ideal for soft samples in danger of being damaged by the tip.

2.1.4.2 *Conductive Atomic Force Microscopy*

Though dynamic modes have surpassed contact mode for most imaging purposes, there are still a number of specialised applications where contact mode must be used – conductive atomic force microscopy (CAFM) is one of these. In CAFM, information on the conductivity of a sample is collected alongside topographic information as a conductive tip is rastered across the surface. By applying a voltage between the sample and the tip, very small currents, as low as picoamps, may be detected at each point, thus building up a conductivity map of the surface. In order to prevent high tip-sample forces but still allow low current detection, special Pt coated tips are used. CAFM has been used to probe the electrical connectivity in single-walled carbon nanotubes,[29] and graphene,[30] and has been used to demonstrate the conductive filaments formed through resistive switching in thin films of TiO_2.[31] As part of this work, a CAFM study of Ag nanowire networks is presented in chapter 4. These results were obtained by Dr Peter Nirmalraj, using a Dimension 3100 (Bruker Corporation) AFM with a CAFM module.

2.2 FABRICATION OF ELECTRICAL CONTACTS ONTO NANOWIRES

Fabrication of electrical contacts onto nanowires requires a complex, multi-step process colloquially known as mix-and-match lithography. While the specific details pertaining to each nanowire shall be discussed in chapter 3, the general procedure will be described here.

Mix-and-match lithography is the combination of fast but lower resolution UV-lithography to form larger (micron to millimetre scale) features, with the significantly slower yet much higher resolution electron beam lithography to fabricate the finer features such as the contacts onto individual nanowires. This combination of techniques utilises the speed of UV-lithography, and the precision and high resolution of EBL.
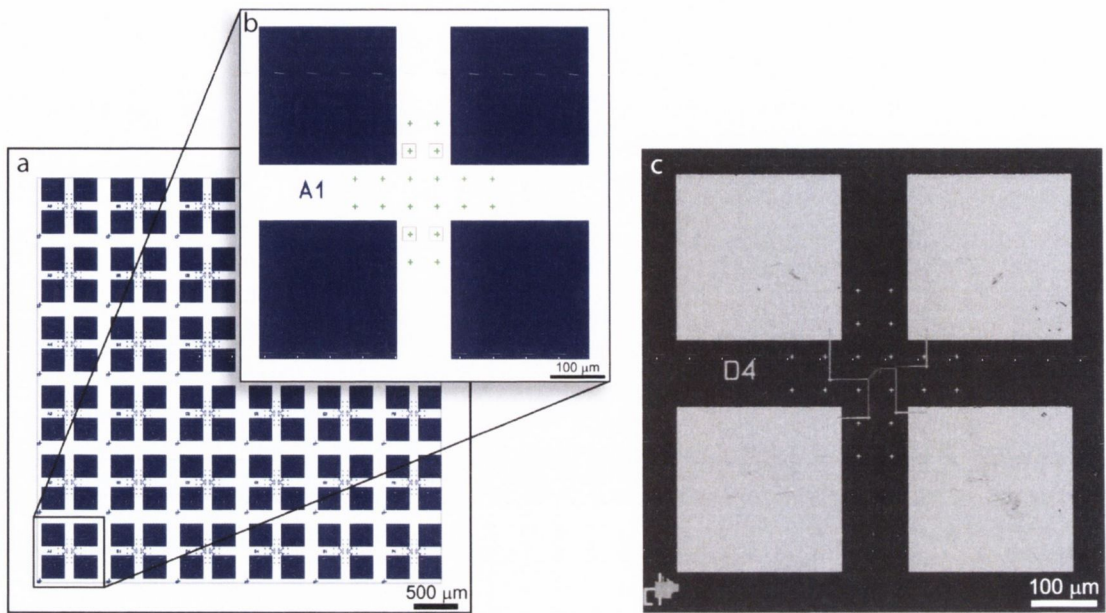
FIGURE 2.13. Photomask design for mix-and-match lithography. (a) 6×6 array of device areas, each containing a 2×2 array of square contact pads (b). (c) SEM image of Au contact pads on SiO_2 substrate. Some finer features fabricated using EBL are visible in the centre of the array.

2.2.1 UV LITHOGRAPHY

UV-lithography operates on the same principles as EBL, with some notable exceptions. Photo-sensitive resist is exposed to the I-line of a mercury vapour discharge lamp (365 nm) through a hard-mask. Masks are typically made of quartz, and are coated in chromium, which is etched selectively producing the desired mask pattern. The resist used in this work is a positive, novolac-type resist. This is a mixture of the phenol formaldehyde (novolac) resin, soluble in aqueous and basic media, with diazonapthoquinone (DNQ) which is insoluble in those media. A photo-induced reaction occurs upon exposure producing an acidic compound, thereby increasing the solubility of the mixture in the basic developer.[11]

In this work, Si wafers with 300 nm of thermally grown SiO_2 were used as substrates for all sample preparation. Wafers were cleaved into 2×2 cm squares. Prior to lithographic processing, all samples were cleaned by sonication in acetone for 5 minutes, followed by an additional sonication in isopropyl alcohol (IPA) for 5 minutes, and dried under N_2 flow. Microposit S1813 (Shipley) positive photo-resist was spun onto substrates and baked according to the protocol below. Samples were then exposed to 365 nm light with an OAI Mask Aligner through a custom designed hard-mask. Figure 2.13 shows an image of the mask design, as well as an SEM image of the resulting device area. The mask produces a 6×6 array of device areas, each containing a 2×2 array of 250 μm square pads, which will act as contacts between the the electrical characterisation system (section 2.4) and the smaller EBL defined contacts. Alignment crosses are also included for the subsequent EBL

step.

The lithography procedure followed in this work is outlined below:

UV lithography recipe

1. Spin S1813 resist at 5000 rpm for 45 sec, with 5 sec ramp at 500 rpm.

2. Soft bake on hotplate at 115°C for 75 sec.

3. Expose at 365 nm for $\sim$ 5.5 sec (dose = 66 mJ cm^{-2}).

4. Develop in MF-319 (Shipley) for 45 sec. Stop in deionised H$_2$O.

The speed at which the resist is spun affects the thickness of the resulting film – 5000 rpm produces a resist thickness of $\sim$ 1.2 μm. A post-apply bake step is required to remove the solvent in the resist prior to exposure. Once the sample is developed, a thin film of Ti/Au (5 nm/35 nm) is deposited onto the sample by electron beam evaporation using a Temescal FC-2000, where Ti acts as an adhesion layer for the Au. The sample is then placed in acetone to remove the remaining resist and expose the metal pattern, a process known as lift-off. The amount of time in acetone required is dependent upon the complexity of the mask design, with closely spaced features requiring longer lift-off times. Non-ideal exposure, possibly arising due to variation in beam intensity or mild sample tilt, can result in underexposure and a failure of fine features to be resolved, or overexposure and a softening of features. In order to calibrate the exposure then, it is prudent to perform a test exposure prior to the main run.

2.2.2 ELECTRON BEAM LITHOGRAPHY

Nanowires are deposited onto the now patterned substrates. The details of this step will be described in the relevant sections in chapter 3. In order to contact individual nanowires, nanowires lying within a device area are first located using optical microscopy. The position of these nanowires relative to the neighbouring alignment marks is determined and used to design the structures that will connect the nanowire to the larger pads. The structures are then drawn using the Raith Multibeam software, which also drives the beam and controls the exposure.

In this work, a bilayer resist is used (Figure 2.14) in order to generate an undercut resist profile, which is ideal for metal deposition. This prevents metal adhering to the resist walls and creating so-called "rabbit ears" on the metal profile. The bilayer resist consists of the copolymer poly(methyl methacrylate - methacrylic acid (8.5%)) (MMA) in ethyl lactate as the bottom layer, and poly(methyl methacrylate) (PMMA) in anisole as the top layer. Figure 2.14 shows an SEM image of a cleaved sample post exposure and development, clearly showing the bilayer structures and undercut profile. Metal contacts on an individual nanowire fabricated using EBL and the bilayer resist are shown in Figure 2.14(c).
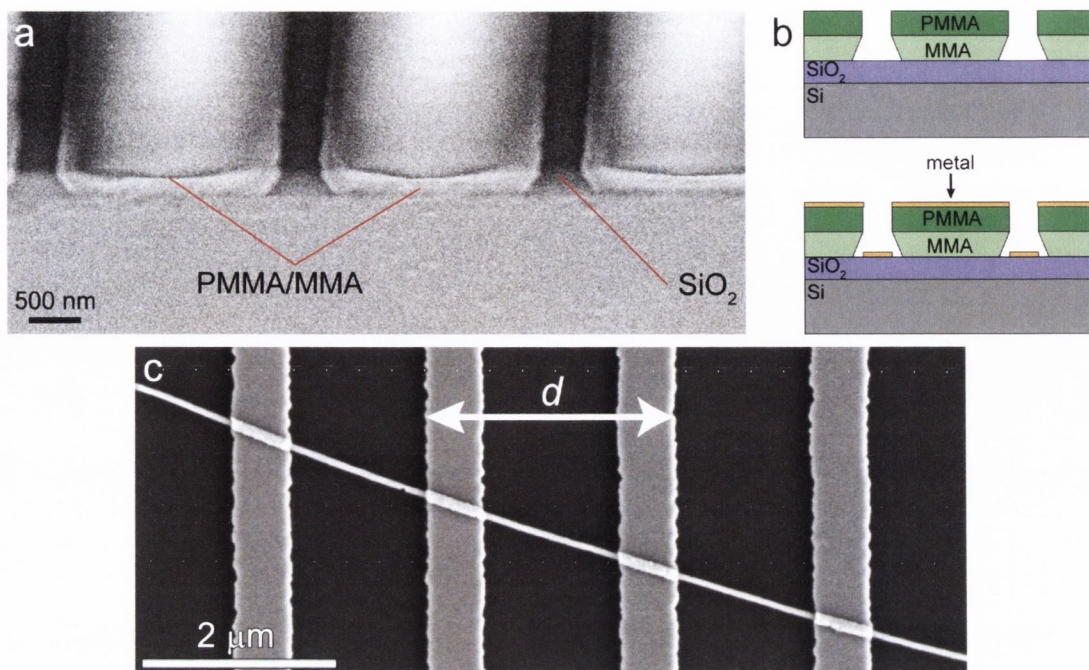
FIGURE 2.14. PMMA/MMA bilayer e-beam resist. (a) SEM image of bilayer resist cross section. (b) Bilayer resist mechanism. (c) SEM image of single nanowire contacted with four 500 nm wide fingers using EBL for resistivity measurements. The inter-electrode spacing, d is shown.

In order to ensure the accuracy of the exposure relative to the design, careful alignment of the sample must be made. This is performed in three steps: compensating for the rotation of the sample, defining a 0,0 origin and defining all translations relative to that point, and finally alignment to predefined structures immediately prior to exposure. Examples of alignment crosses may be seen in Figure 2.13(b) and (c). Once aligned, the Raith software then rasters the beam according to the designs. As discussed in section 2.1.2, choice of accelerating voltage is key to obtaining high resolution exposures. Another parameter available to the user is the choice of aperture size. Smaller apertures produce higher resolution features, however the current drops off correspondingly, increasing the exposure times.

The recipe followed for correct exposure of the bilayer resist is as follows:

Bi-layer resist recipe

1. Spin MMA EL9 at 6000 rpm for 45 sec, with 5 sec ramp at 500 rpm.

2. Soft-bake on hotplate at 180°C for 120 sec.

3. Spin PMMA A3 at 3000 rpm for 45 sec, with 5 sec ramp at 500 rpm.

4. Soft-bake on hotplace at 180°C for 180 sec.

5. Expose with the following parameters:

> - *Accelerating voltage:*   10 kV
>
> - *Aperture size:*   20 μm
>
> - *Dose:*   130 μC cm^{-2}
>
> 6. Develop in MIBK:IPA 1:3 for 60 sec. Stop in IPA.

2.3 NANOWIRE NETWORK FABRICATION

The merits of nanowire networks were discussed in chapter 1; here the methods used to fabricate such networks will be discussed. The formation of nanowire networks is as important as any other step in the preparation of a working device. How the wires are connected to each other, whether the connections are evenly distributed yet random, or if there is a tendency to aggregate is vital, as it directly affects the connectivity and thus the electrical properties of the network.

Numerous methods have been used in the literature to fabricate networks, including doctor blading,[32,33] spin coating,[34] self-assembled growth,[35] drop casting,[36] vacuum filtration,[37,38] and spray deposition.[39–41] Methods such as doctor blading and drop casting are highly unreliable for forming highly random, uniform networks on any scale due to effects such as coffee-staining. Spin-coating and vacuum filtration methods have demonstrated highly uniform networks, however these techniques are not suitable for scale up to industry, while self-assembled growth is still purely an experimental technique. Spray deposition has been proven to produce highly uniform, random networks over large areas, suitable for industrial scale-up, and is the method used in this work to fabricate networks of nanowires.

Spray deposition is a simple technique whereby a dilute, colloidal dispersion of the desired nanomaterial is sprayed onto a surface some centimetres away by a spray gun. The dispersion, typically based on a volatile solvent, is atomised into microscopic droplets by a large pressure differential created at a small aperture, less than 1 mm in diameter. The atomised dispersion is accelerated toward the target surface by a high back pressure, nominally 1.5–3 bar. The volatile droplets evaporate immediately upon impact with the surface, preventing undesirable effects such as coffee-staining or aggregation of the nanomaterial, forming truly randomly oriented networks. In this work, a 3-axis robotic gantry, developed in collaboration with Hewlett Packard, was used to fabricate uniform networks over large scales (see Figure 2.15), however hand spraying may also be performed on smaller area samples with excellent results. To build the robotic spraying system, a Janome JR2300N desktop robot was fitted to hold an artist's spray gun (Infinity, Harder & Steenbeck), such that the spray lever on the gun could be pneumatically operated (Figure 2.15(b)). The rate of impingement may be controlled by adjusting the position of a sharp needle relative to the
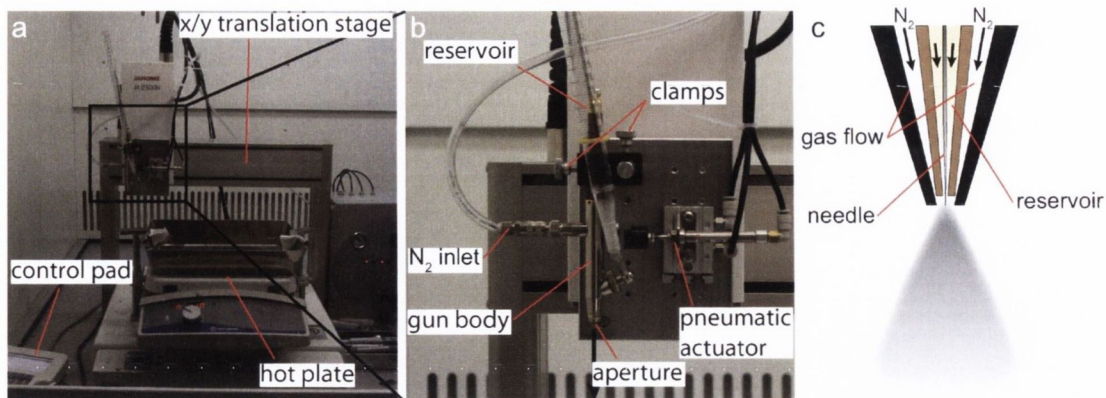
Figure 2.15. Robotic spraying system. (a) 3-axis robot (Janome) fitted with an Infinity spray gun (Harder & Steenbeck). A hotplate was also built into the system to allow less volatile solvents to be sprayed. (b) Detailed view of the gun. A pneumatic actuator operates the gun, while a graduated reservoir allows spray volume to be accurately measured. A $600\,\mu$m nozzle size was used, and the N_2 backing pressure was nominally 2.75 bar (40 psi). (c) Schematic of spray mechanism.
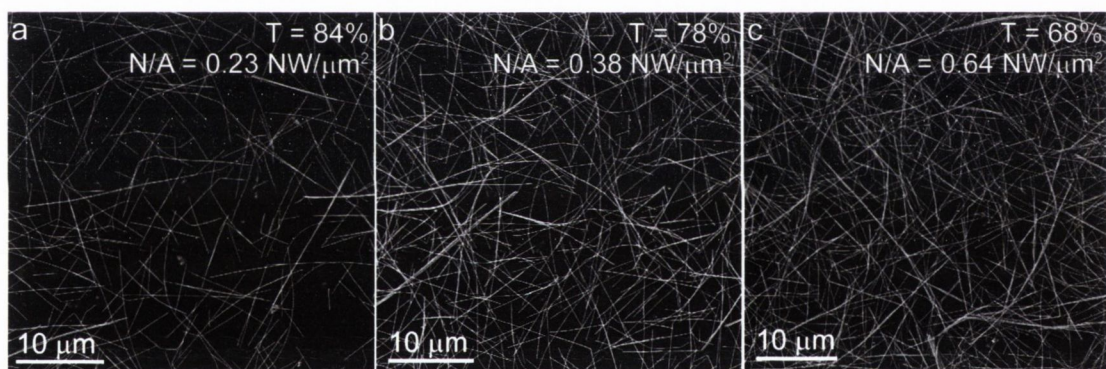
Figure 2.16. SEM images of sprayed Ni nanowire networks for three network densities. The transmittance and nanowire number density is displayed for each network.

reservoir aperture (Figure 2.15(c)), and is capable of spraying continuously for extended periods of time over large areas ($> 600\,$cm^2).

In this work, the density of a random network is characterised by two parameters: the nanowire number density (N/A) in NW$\,\mu$m^{-2}; and the percentage transmittance of 550 nm light (T), measured using a UV-vis spectrometer. Figure 2.16 shows networks of Ni nanowires fabricated via the spray deposition technique just described for three different network densities. For each batch of nanowires used in this work, a spray calibration was performed, where the transmittance was measured as a function of volume sprayed. This was then used to determine the approximate transmittance for all subsequent networks. It has been shown that by measuring T, one can calculate the number density of nanowires if the dimensions of the nanowires are known.[37,40] Equation (2.2) relates T to the network

thickness, t, by the impedance of free space, Z_0, and the network optical conductivity, σ_{op}.

$$T = [1 + \frac{Z_0}{2}\sigma_{op}t]^2 \tag{2.2}$$

The nanowire number density is then related to the network thickness through the nanowire dimensions, r_{NW} and L_{NW}, and the ratio of the network density, ρ_{net}, to the density of the bulk material, ρ_{bulk}, via:

$$\frac{N}{A} = \frac{\rho_{net}}{\rho_{bulk}}\frac{t}{\pi r_{NW}^2 L_{NW}} \tag{2.3}$$

De et al. have shown that for a Ag nanowire network $\rho_{net}/\rho_{Ag} = 0.04$.[37]

Once a network is formed, in order to investigate the electrical properties, metallic contact must be made. This is achieved by evaporating metal contact pads on top of the network, which are then contacted by micro-needles (see section 2.4). Unlike single nanowires, conventional lithographic methods are not effective at making contact to networks. Nanowires in flush contact with a substrate experience strong Van der Waals forces adhering them to the surface, however as the network density increases, the number of nanowires making flush contact with the substrate is greatly reduced. The majority of nanowires are thus only weakly held to the substrate through Van der Waals forces. The lithographic process, and in particular the metal lift-off step, then has a strong tendency to remove these nanowires, often breaking connective paths in an otherwise percolative network. In order to circumvent this problem, a shadow mask technique was used. Shadow masking utilises a laser-drawn stencil mask placed in flush contact with a surface, through which metal is then evaporated. Metal is then deposited only through the laser-cut holes, allowing metallic contact pads to be placed without the use of lithography or polymeric resists. Shadow-masking is significantly faster than UV-lithography, as it is a single-step process, and a single mask may be used multiple times. Due to diffusion of the metallic vapour, the resolution of shadow masking is limited and features smaller than $10\,\mu\text{m}$ are unattainable. An image of the mask design used in this work, alongside an SEM image of a $20 \times 20\ \mu\text{m}$ contacted network is shown in Figure 2.17.

The size of a given network is defined by the ratio of the inter-electrode distance, D, of the contacting electrodes, and the average length of the nanowires being examined, L_{NW}. In all cases, a square network geometry is employed, such that the inter-electrode distance is equal to the electrode width, W. This relationship breaks down slightly at smaller D values due to the diffusion of metal at the shadow mask edge, reducing the value of D. As the scaling behaviour of networks is examined in chapters 4 and 5, the definition of the network size is of critical importance. Hence the networks are normalised in this manner to account for their geometry, in order to focus on the behavioural differences stemming from changes in the network connectivity.
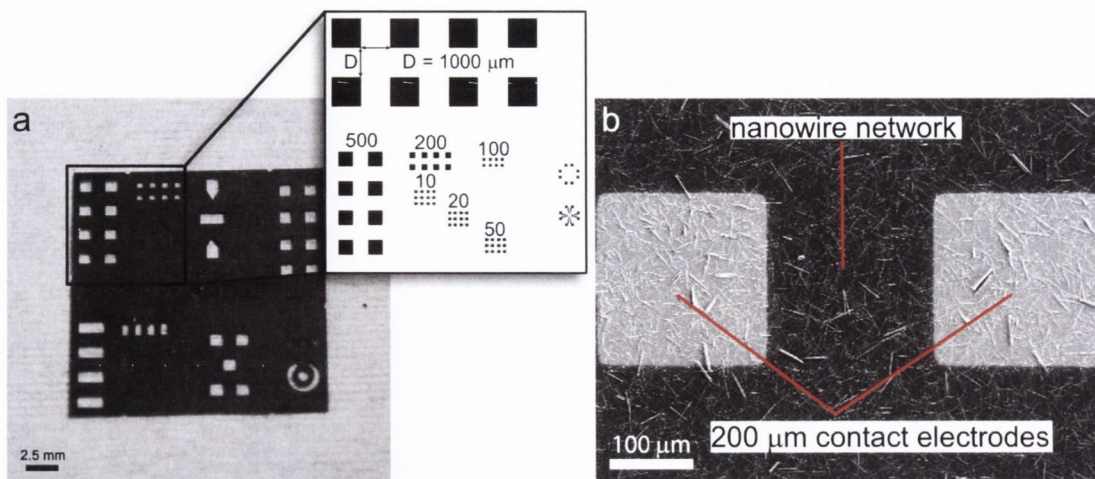
FIGURE 2.17. Electrically contacting nanowire networks. (a) Image of shadow mask used to make electrical contact to nanowire networks, and design showing square electrode and their corresponding sizes. Electrode spacings as small as 10 μm are possible. (b) SEM image of contacted 200 μm nanowire network.

2.4 ELECTRICAL CHARACTERISATION

The electrical characterisation of devices is the primary investigative method used in this thesis. Both AC and DC electrical measurements are performed on single nanowire junctions in chapter 3, while solely DC methods are used to study networks of both Ag and Ni nanowires in chapters 4 and 5. This section shall focus on the equipment and methods used to perform these measurements.

2.4.1 DC ELECTRICAL MEASUREMENTS

Two electrical characterisation systems were used in this work. System I, an image of which is shown in Figure 2.18(a) and schematically shown in Figure 2.19(c), consists of a suite of source-measure units (SMUs), a current pre-amplifier, and two multimeters. The system is controlled by Labview software via GPIB connection to a central computer. Coaxial cables connect the instruments to the grounding box, and from there are connected to a Karl Suss PM-8 probe station. Due to a limitation of the current pre-amplifier, the maximum measurable current of this system is 7 mA. System II is a much more advanced system, consisting of the Keithley 4200 Semiconductor Characterisation System (SCS) (Figure 2.18(b) and (c)). Four SMUs, containing two current pre-amplifiers, as well as capacitance-voltage units (CVUs) for AC measurements, and two nanosecond pulse meters (PMUs) are housed within the unit, also containing a PC running Keithley proprietary software to control and drive the instruments. Very low noise triaxial (triax) cables connect the SMUs to the probe station, while coaxial SMA cables are used for both CVU and PMU operation. At the highest sensitivity amplification, currents noise levels as low as 10 fA may be achieved with this system.
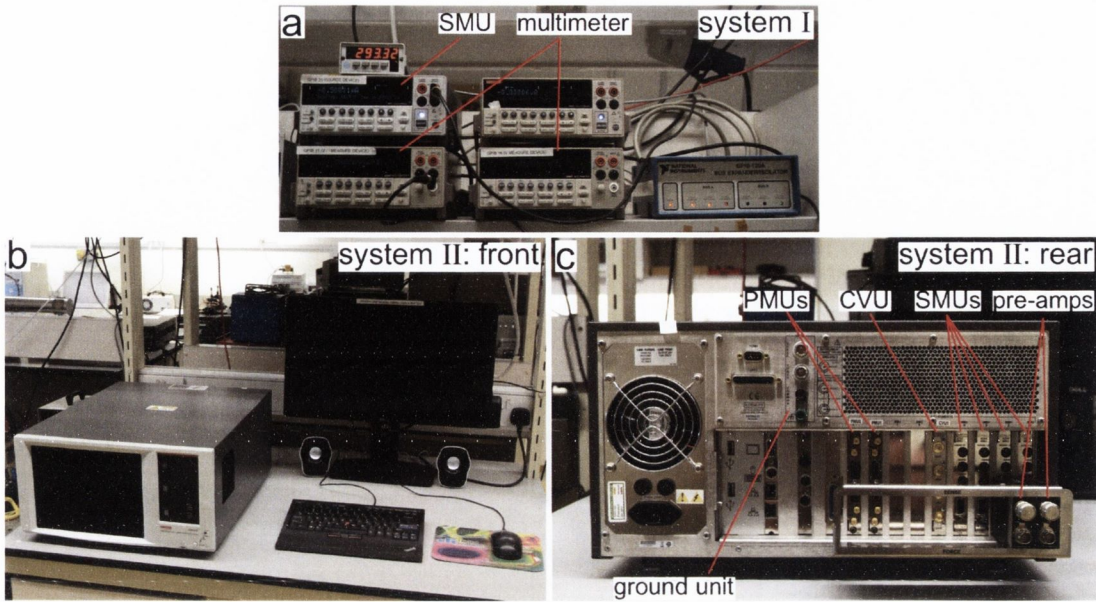
FIGURE 2.18. Images of electrical characterisation systems used in this work. (a) System I, consisting of an SMU, two multimeters and a current pre-amplifier (not shown). (b) System II: Keithley 4200 SCS, front view, and (c) rear view. Four SMUs, two pre-amplifiers, one CVU, and two PMUs are housed within the unit.
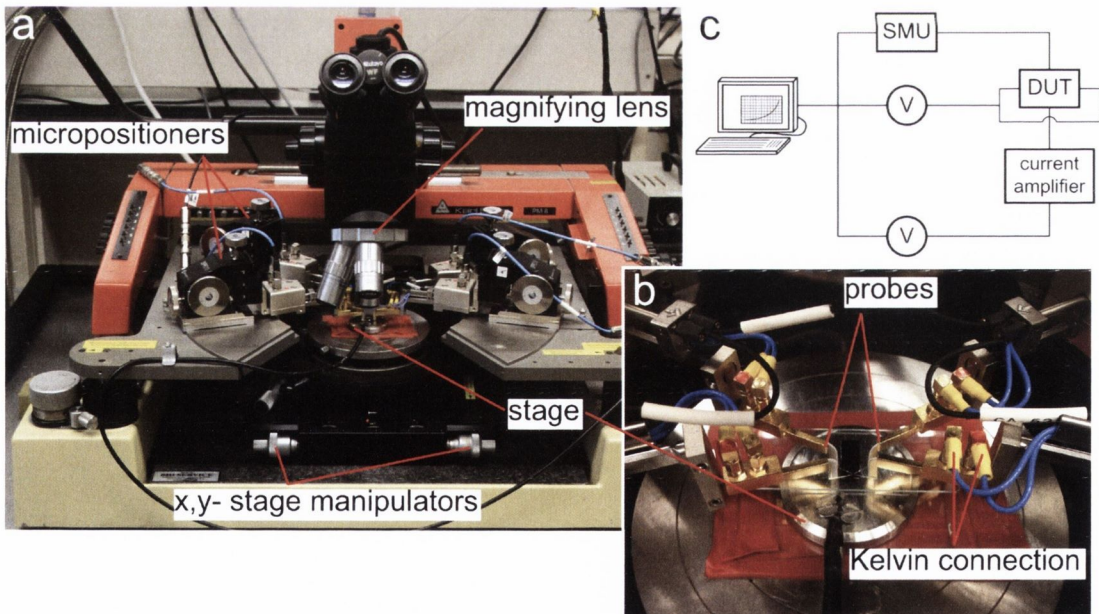
FIGURE 2.19. Electrical characterisation system. (a) A Karl Suss PM-8 probe station makes electrical contact to samples via Cascade Microtech micropositioners and micro-needles (b). (c) Schematic of system I. A computer running Labview software instructs a source measure unit (SMU) to drive current/voltage across the device under test (DUT). The current signal is then amplified, measured, and read by the computer. An additional multimeter is available for 4-probe measurements.
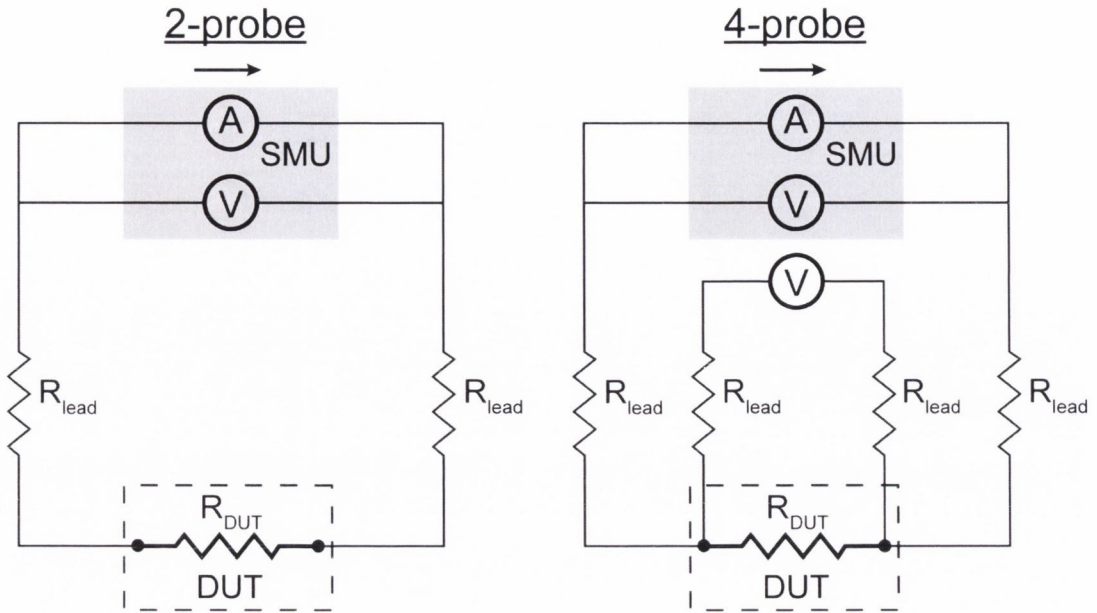
FIGURE 2.20. Equivalent circuits demonstrating both 2-probe and 4-probe measurement regimes. By measuring the voltage drop across the DUT, the contact resistance is removed from the measurement.

Both system I and II are connected to a Karl Suss PM-8 probe station (Figure 2.19(a)), where electrical contact to samples is made. The probe station houses four micropositioners (Cascade Microtech) with tungsten micro-needles (Figure 2.19(b)), allowing for accurate positioning and gentle contact to samples. The radius of the microneedles is nominally $20\,\mu$m. The signal from each probe may be split a few centimetres from the contact point for Kelvin measurements, reducing the noise levels even further.

Resistance measurements may be performed in either a 2-probe geometry, or a 4-probe geometry. 2-probe measurements employ a single SMU to drive either current/voltage across a sample, determining the resistance by the ratio of the voltage supplied to the current measured. For high impedance samples this produces accurate measurements, however for low impedance samples ($\leq 10\,$kΩ), contact resistance will have an appreciable contribution to the measured resistance. In order to remove the effect of contact resistance and accurately measure the resistance of a low impedance sample, 4-probe measurements must be made. Figure 2.20 schematically illustrates the differences between the two measurement regimes. By sourcing current across the outer most contacts, and measuring the corresponding voltage drop across the inner contacts, the contact resistance can be effectively removed. The resistivity of the material may then be calculated based on the distance between the inner contacts, d and cross sectional area of the material, A, according to

$$\rho = \frac{RA}{d} \tag{2.4}$$

Kolesnik et al. showed that for nanoscale measurements of resistivity, it is appropriate to

take the value of d to be the distance from the outer edges of the inner contacts, as shown in Figure 2.14(c).[42]

Finally, equation (2.4) may be rewritten in terms of the film thickness, t, as

$$R = \frac{\rho}{t}\frac{d}{W} \tag{2.5}$$

where the term ρ/t is known as the sheet resistance, R_s, and has units $\Omega/\square$. R_s is a common parameter used to characterise the resistance of thin films.

2.4.2 AC ELECTRICAL MEASUREMENTS: IMPEDANCE SPECTROSCOPY

Sweeping a DC bias across a sample provides a simple relationship between the voltage and the current response. If the sample is metallic, this response will follow Ohm's law

$$R = \frac{V}{I} \tag{2.6}$$

where R is the total resistance of the circuit. Within this resistance value is contained the sample resistance, as well as the contact and lead resistances. In order to isolate the sample resistance 4-probe measurements must be made, as outlined in section 2.4.1. However no information is gathered about other linear circuit components such as capacitors or inductors. In order to measure the response of these elements, AC measurements must be made. Under an AC bias, the total electrical impedance is then the sum:

$$Z = R + jX \tag{2.7}$$

where R is the sample resistance, and X the sample reactance – the opposition of a capacitor/inductor to changes in the voltage/current respectively. By measuring Z as a function of the applied AC frequency, information regarding the contribution of resistive, capacitive, and inductive components may be extracted. This is a technique known as impedance spectroscopy, and is a powerful technique used to analyse complex samples and extract meaningful information about individual components, ultimately allowing the user to determine an equivalent circuit for otherwise highly complex physical phenomena.[43] In this work, impedance spectroscopy is used to investigate junctions of Ag and Ni nanowires, with the aim of learning more about the switching phenomena that occur at these interfaces.

In its simplest form, impedance spectroscopy measures the total impedance of a circuit, Z, (or the modulus, $|Z|$), and the phase angle, θ, as a function of the frequency of the applied signal. In the general form, Ohm's law looks like

$$v(t) = i(t)R \tag{2.8}$$

which for the case of a resistor, results in equation (2.6). For the case of a capacitor however,

we get the time dependent relationship

$$i_C(t) = C \frac{d\,v_C(t)}{dt} \tag{2.9}$$

As the voltage signal is $v(t) = V_p \sin(\omega t)$, the ratio of the voltage and current is then:

$$\frac{v(t)}{i_C(t)} = \frac{\sin(\omega t)}{\omega C \sin(\omega t + \frac{\pi}{2})} \tag{2.10}$$

which may be written as:

$$Z_{capacitor} = \frac{1}{j\omega C} \tag{2.11}$$

Equation (2.10) states that the phase angle between the current and voltage signals in a capacitor is -90 degrees. Similarly, for an inductor:

$$Z_{inductor} = j\omega L \tag{2.12}$$

where the phase angle is +90 degrees.

Following from equation (2.7), the measured impedance of a circuit is equal to the sum of the various resistances and reactances present. For a series LCR circuit, such as that shown in Figure 2.22, this is:

$$|Z| = \sqrt{R^2 + \left((\omega L)^2 - \left(\frac{1}{\omega C} \right)^2 \right)} \tag{2.13}$$

where the phase angle is:

$$\theta = \tan^{-1}\left(\frac{X}{R} \right) = \tan^{-1}\left(\frac{X_L - X_C}{R} \right) \tag{2.14}$$

For an RC parallel circuit, such as that in Figure 2.22, the situation is more complex:

$$|Z| = \sqrt{\left(R_s + \frac{R_p}{1 - \left(\omega C R_p \right)^2} \right)^2 + \left(\frac{\omega C R_p}{1 - \left(\omega C R_p \right)^2} \right)^2} \tag{2.15}$$

and

$$\theta = \tan^{-1}\left(\frac{\omega C R_p}{R_s \left(1 - \left(\omega C R_p \right)^2 \right) + R_p} \right) \tag{2.16}$$

where R_s and R_p are the series and parallel resistances, respectively.

By fitting impedance data to complex equations such as these, the parameters R_s, R_p, C etc. may be extracted, thereby providing valuable information about a system. In order to determine an equivalent circuit and extract value out of impedance data, there are a number of ways of plotting data which will give indications as to the mechanisms at play within a system. Figure 2.21 shows two commonly used plots for the example of a simple
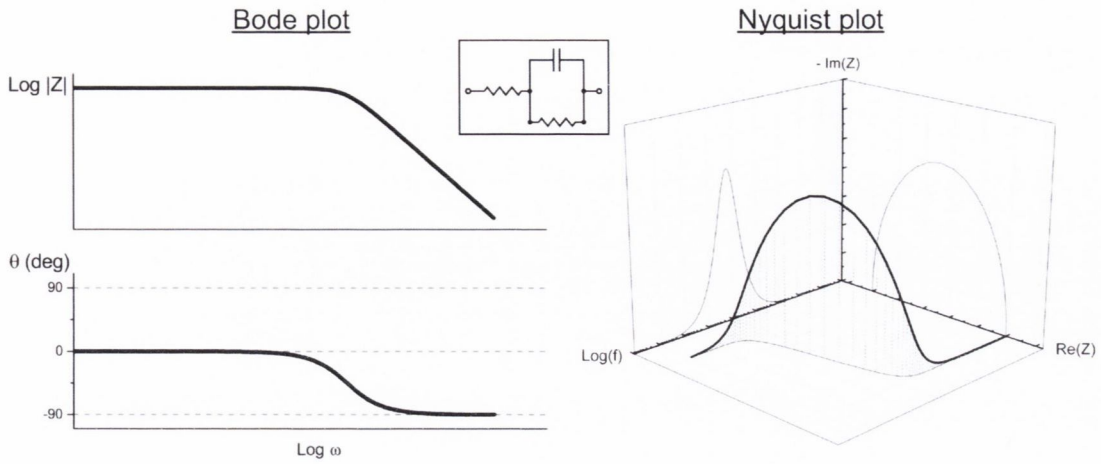
FIGURE 2.21. Impedance data plots for an RC parallel circuit. The Bode plot: $|Z|$ and θ plotted as a function of $\log \omega$. The Nyquist plot: the negative imaginary impedance, $-\mathrm{Im}(Z)$, is plotted as a function of the real impedance, $\mathrm{Re}(Z)$. Semicircular plots are characteristic of RC parallel circuits. The 3D projection plot shown here also demonstrates $\mathrm{Re}(Z)$ vs. $\log \omega$ and $-\mathrm{Im}(Z)$ vs. $\log \omega$ plots.
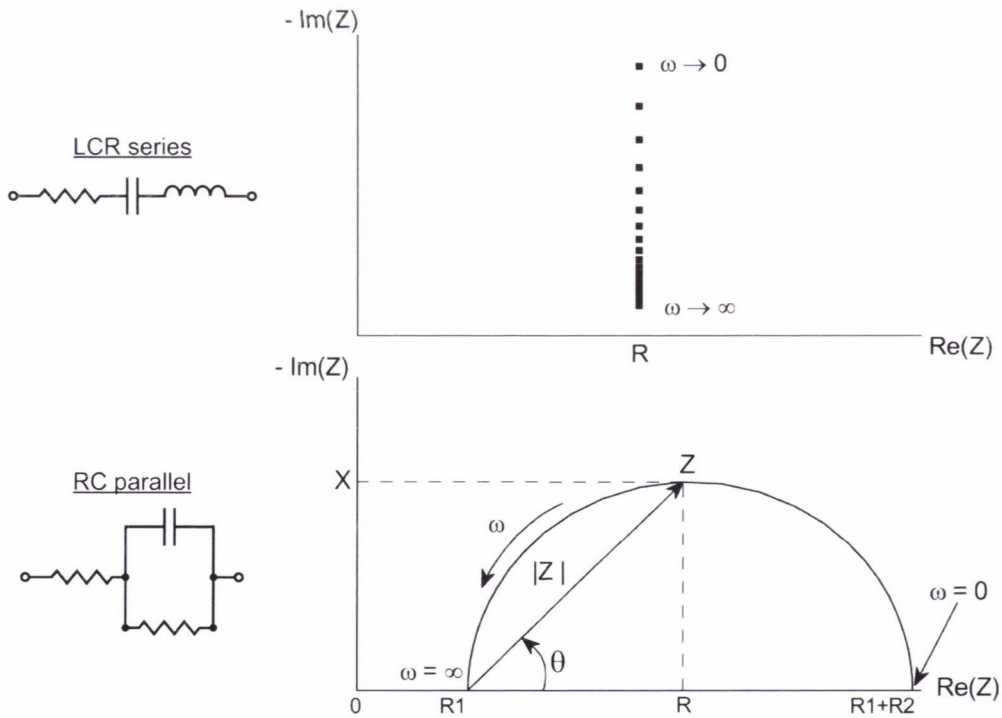
FIGURE 2.22. Nyquist plot for LCR series circuit and an RC parallel circuit. The shape of the plot is a strong indicator as to the form of the equivalent circuit.

RC parallel circuit: the Bode plot, and the Nyquist plot. Bode plots display $|Z|$ and θ against frequency, ω. As stated above, the phase angle is -90°, 0°, or +90° for capacitors, resistors, and inductors respectively. Thus the Bode plot gives users a simple way to identify if a system is resistive, capacitive, or inductive, and at what frequencies these traits become dominant. Nyquist plots display the imaginary component (X) of the impedance against the real component (R), and have characteristic shapes depending on the equivalent circuit. In the example shown, a semicircle is formed, characteristic of RC parallel circuits, while RC series circuits display a single vertical line at R (Figure 2.22).

The AC electrical characterisation in this work was performed using the capacitance voltage capabilities of system-II. The available frequency range of this unit is 1 kHz – 10 MHz, however due to limitations of the electrical characterisation system at high frequencies, the usable range is reduced to 1 kHz – 1 MHz. Due to the complexity of equations (2.15) and (2.16), experimental data is fitted using a complex non-linear least squares fitting program, developed by James Ross MacDonald, called LEVM.[44] Further details regarding the implementation of these techniques to the measurement of single nanowire junctions is provided in detail in chapter 3.

2.5 CONCLUSION

In this chapter, the working principles of the many techniques used in this thesis have been described in detail. Scanning electron microscopy and atomic force microscopy are both ubiquitous tools in the field of nanoscience, providing users with multiple imaging regimes and methods of sample characterisation including elemental analysis (EDX) and conductivity analysis (CAFM). The helium ion microscope as a commercial technology is still in its infancy, however its demonstrated capabilities make it an exciting prospect for the future. The methods used to fabricate contacts on single nanowires as well as large networks have both been described, as have the electrical techniques used to measure the resulting devices. Chapter 3 that follows is the first of three experimental chapters in this thesis, and describes the measurement of the junction resistance for junctions of both Ag and Ni nanowires, discussing the implications of these measurements for transparent conductor research.

REFERENCES

[1] KNOLL, M. and RUSKA, E., *Zeitschrift für Physik* **1932**, *78*, 318–339.

[2] WATT, I. M., *The principles and practice of electron microscopy*, Cambridge University Press, **1997**.

[3] EVERHART, T. and THORNLEY, R., *Journal of scientific instruments* **1960**, *37*, 246.

[4] GRIFFIN, B., JOY, D., and MICHAEL, J., *Microscopy and Microanalysis* **2009**, *15*, 46–47.

[5] COLVIN, J., in *Proc. 16th Int. Symp. Testing and Failure Analysis*, page 331.

[6] LEE, J. C., CHEN, C., SU, D. ET AL., *Microelectronics Reliability* **2002**, *42*, 1707–1710.

[7] SEILER, H., *Journal of Applied Physics* **1983**, *54*, R1–R18.

[8] HAUG, E. and NAKEL, W., *The Elementary Process of Bremsstrahlung*, World Scientific lecture notes in physics, World Scientific, **2004**.

[9] MOLLENSTEDT, G. and SPEIDEL, R., in *Third Symposium on Electron Beam Processes (SEBP), 1961*, volume 3, pages 340–357.

[10] BROERS, A., MOLZEN, W., CUOMO, J. ET AL., *Applied Physics Letters* **1976**, *29*, 596–598.

[11] LANDIS, S., *Lithography*, John Wiley & Sons, **2013**.

[12] CHANG, T., *Journal of Vacuum Science & Technology* **1975**, *12*, 1271–1275.

[13] STEPANOVA, M. and DEW, S., *Nanofabrication: Techniques and Principles*, Springer, **2011**.

[14] HOVINGTON, P., DROUIN, D., and GAUVIN, R., *Scanning* **1997**, *19*, 1–14.

[15] DROUIN, D., *CASINO Monte Carlo Simulation Software*, http://www.gel.usherbrooke.ca/casino/.

[16] WARD, B. W., NOTTE, J. A., and ECONOMOU, N. P., *Journal of Vacuum Science and Technology B* **2006**, *24*, 2871–2874.

[17] MÜLLER, E. W., *Journal of Applied Physics* **1956**, *27*, 474–476.

[18] SCIPIONI, L., STERN, L., NOTTE, J. ET AL., *Advanced Materials and Processes* **2008**, *166*, 27.

[19] ECONOMOU, N. P., NOTTE, J. A., and THOMPSON, W. B., *Scanning* **2012**, *34*, 83–89.

[20] RAMACHANDRA, R., GRIFFIN, B., and JOY, D., *Ultramicroscopy* **2009**, *109*, 748 – 757.

[21] BELL, D. C., *Microscopy and Microanalysis* **2009**, *15*, 147–153.

[22] VAN DER DRIFT, E. and MAAS, D. J., *Helium ion lithography*, Springer, **2012**.

[23] ALKEMADE, P. F., KOSTER, E. M., VAN VELDHOVEN, E. ET AL., *Scanning*

2012, *34*, 90–100.

[24] ZHOU, Y. and LOH, K. P., *Advanced Materials* **2010**, *22*, 3615–3620.

[25] BINNIG, G., QUATE, C. F., and GERBER, C., *Physical Review Letters* **1986**, *56*, 930–933.

[26] ERLANDSSON, R., OLSSON, L., and MARTENSSON, P., *Physical Review B* **1996**, *54*, R8309–R8312.

[27] ANDO, T., *Microscopy* **2013**, *62*, 81–93.

[28] EATON, P. and WEST, P., *Atomic Force Microscopy*, Oxford University Press Inc., **2010**.

[29] NIRMALRAJ, P. N., LYONS, P. E., DE, S. ET AL., *Nano Letters* **2009**, *9*, 3890–3895.

[30] NIRMALRAJ, P. N., LUTZ, T., KUMAR, S. ET AL., *Nano Letters* **2011**, *11*, 16–22.

[31] CHOI, B. J., JEONG, D. S., KIM, S. K. ET AL., *Journal of Applied Physics* **2005**, *98*, 033715–.

[32] HUANG, Y., DUAN, X., WEI, Q. ET AL., *Science* **2001**, *291*, 630–633.

[33] LIU, C.-H. and YU, X., *Nanoscale Res. Lett* **2011**, *6*, 75.

[34] CHUNG, C.-H., SONG, T.-B., BOB, B. ET AL., *Nano Research* **2012**, *5*, 805–814.

[35] STIEG, A. Z., AVIZIENIS, A. V., SILLIN, H. O. ET AL., *Advanced Materials* **2012**, *24*, 286–293.

[36] LEE, S., CHAE, S., CHANG, S. ET AL., *Applied Physics Letters* **2008**, *93*, 212105.

[37] DE, S., HIGGINS, T. M., LYONS, P. E. ET AL., *ACS Nano* **2009**, *3*, 1767–1774.

[38] BERGIN, S. M., CHEN, Y. H., RATHMELL, A. R. ET AL., *Nanoscale* **2012**, *4*, 1996–2004.

[39] SCARDACI, V., COULL, R., LYONS, P. E. ET AL., *Small* **2011**, *7*, 2621–2628.

[40] NIRMALRAJ, P. N., BELLEW, A. T., BELL, A. P. ET AL., *Nano Letters* **2012**, *12*, 5966–5971.

[41] KIM, T., CANLIER, A., KIM, G. H. ET AL., *ACS applied materials & interfaces* **2013**, *5*, 788–794.

[42] KOLEŚNIK, M. M., HANSEL, S., LUTZ, T. ET AL., *Small* **2011**, *7*, 2873–2877.

[43] BARSOUKOV, E. and MACDONALD, J. R., *Impedance spectroscopy: theory, experiment, and applications*, John Wiley & Sons, **2005**.

[44] MACDONALD, J. R., *LEVM Complex Nonlinear Least Squares Fitting Program*, http://www.jrossmacdonald.com/levminfo.html, **2012**.

3

RESISTANCE OF SINGLE Ag & Ni NANOWIRE JUNCTIONS

This thesis aims to examine the connectivity of nanowire networks, and central to this is an understanding of the nanowire-nanowire junction. Junctions are critical connecting points in a network, and thus not only control the resistance of the film, but also the network connectivity. Additionally, a full and complete understanding of the junctions is essential in order to generate accurate models to describe these systems, which thus far in the literature have been inconsistent. This chapter will present electrical measurements performed on both Ag and Ni nanowire junctions, measuring accurately the critical parameter, R_{jxn}, the junction resistance. Impedance spectroscopy measurements of these single nanowire junctions will also be discussed.

3.1 MOTIVATION

Explored in chapter 1, research into nanowire networks for various technological applications continues to grow year after year. Networks show promise for transparent conductors, artificial skin technology, and have been demonstrated in many sensing applications, due to their inherent thin film nature, creating flexible and transparent materials at low cost with relative ease of fabrication. Ag nanowire networks are widely regarded as the successor to indium tin-oxide (ITO) as a high performance transparent conductor, not only matching the properties of ITO by achieving sheet resistances of $10\,\Omega/\square$ at 90% transmittance, but also providing mechanical flexibility that will be essential for next generation electronics.

It is likely that networks will require different properties for different applications. For example, some applications may require extremely high transmittance values while specific sheet resistance is not as critical, or vice versa, or certain applications may benefit from a diffusive transparent conductor, either for practical or aesthetic purposes, for example in solar cells. It is impractical to conduct a research project for each individual application, particularly if budget is a limitation. Rather, a more efficient system would be a central

database which could be drawn upon to design a material to a client's specifications. To achieve such a system, a full and complete understanding of a network will be required, such that a computer model may generate the required material based on the desired parameters. A number of studies have already been undertaken determining relationships between physical properties (nanowire length/diameter) and parameters such as sheet resistance, optical transmittance, or clarity of the resulting film.[1–4]

To complete the picture, the local nanoscale interactions, such as those at the junctions, must be correlated with the macroscale properties such as sheet resistance. Already discussed in chapter 1, a number of studies have been performed with this in mind, focusing on a top-down simulation approach. Lee et al. find their simulations map onto experimental results for a range of R_{jxn} values from 1 to 100 Ω.[5] They reason that at higher network densities, the number of junctions per nanowire is greater than 1, and therefore the network is able to choose the lowest resistance junctions, producing a false impression of the average. While this reasoning is sound, there are still a number of issues with this conclusion. Firstly, no direct measurement of R_{jxn} is performed, and thus there is no way to verify the results of the simulation. Additionally, it is not specified whether the measurements made were 4-probe or 2-probe. Not accounting for the contact resistance in such low impedance measurements would have a significant impact on the sheet resistance obtained, and is thus a vital piece of information.

Mutiso et al. performed a comprehensive study combining simulation of random 2-D rod networks with experimental sheet resistance measurements, and find that an average R_{jxn} value of 2 kΩ fits the experimental data most accurately.[6] These results represent a valuable contribution toward the generation of a materials-by-design approach, particularly demonstrating the value of combined experiment and simulation. However, there are a number of limitations to such a study. In particular, the resistance contribution of each nanowire was set to be zero, assuming that the junction resistance was much larger and therefore would have a much greater influence on the sheet resistance of the film. Assuming a network size of several hundred microns to several millimetres, the total length of the conducting path is significant, and therefore the resistance contribution from the nanowires themselves cannot be overlooked. It is likely that this is the main reason for the difference in R_{jxn} values obtained in this study and those obtained by Lee et al. in 2008.

From these two studies, it is clear that there is currently insufficient understanding of the nanowire junction properties, and that top-down approaches to measuring R_{jxn} have failed to provide consistent results. It is therefore essential to obtain direct measurements of the nanowire junctions, which may then be combined with simulation techniques, such as those used by Mutiso et al., to generate a complete network model. A number of publications have attempted to address this problem, measuring the resistance of individual nanowire junctions.[7–9] With the exception of the study by Hu et al. in 2010, these single junction measurements have all been 2-probe measurements, and thus do not provide an accurate measurement of R_{jxn}. Additionally, the measurement performed by Song et al. is the only one to account for the resistance contribution of the nanowire length, which is shown in

TABLE **3.1.** Summary of Ag nanowire junction resistance values in literature

Author	Year	R_{jxn} (Ω)	Method
Lee et al.	2008	1–100	fitting simulations to experimental R_S values
Hu et al.	2010	450	4-probe measurement of single junction
Garnett et al.	2012	$\sim 1 \times 10^4$	2-probe measurement of single junction
Mutiso et al.	2013	$\sim 2 \times 10^3$	fitting simulations to experimental R_S values
Song et al.	2014	185	2-probe measurement of single junction

this work to be of equal or greater magnitude to that of the junction itself.

The junction resistance value reported in each of the studies mentioned thus far has been summarised in table 3.1. It is clear that not only do the top-down measurements produce inconsistent results, but direct measurements of single junctions have also been inconsistent to date, with only one study performing 4-probe measurements to remove contributions from the contact resistance. Additionally, it appears that only a single value was measured in each study, again placing the results into question. The work presented in this chapter attempts to address this issue by performing accurate measurements of single Ag nanowire junctions under a number of preparation conditions, providing the first instance of an accurate R_{jxn} distribution.

3.1.1 BEYOND Ag: Ni NANOWIRES

It has been established that an understanding of the nanowire junctions is critical to the characterisation of a nanowire network, and that this may lead to a materials-by-design approach. Once this understanding has been developed, it is natural to begin to manipulate the junction in order to add new properties to the network, potentially adding new levels of functionality into a nanowire network and creating applications not previously thought possible. This is the motivation behind extending the study beyond Ag and investigating the properties of junctions of Ni nanowires.

As discussed in chapter 3, one limitation of current nanowire based thin film technologies is their tendency to degrade over time when exposed to ambient conditions, increasing the resistance of the film and thereby rendering a device obsolete. One approach to solving this problem is to specifically design materials to resist oxidation/degradation. Both Rathmell et al. and Chen et al. propose a similar approach to solving this problem, by specifically designing and fabricating protective coatings onto copper nanowires. [10,11] The resulting films display significant resistance to oxidation compared to either pure Cu or pure Ag nanowires at elevated temperatures, while retaining much of the conductivity of the pure Cu network. A different approach to solving the problem of film degradation however, is to take advantage of the natural oxidation layers displayed by many materials,

and fabricate connected networks of passivated nanowires. One such material displaying a native passivation layer is Ni. A self-limiting layer of NiO, 5-10 nm in thickness, forms natively on the surface of Ni under ambient conditions, resulting in a Ni/NiO core-shell structure when nanowires of Ni are exposed to air. As already shown by He et al. this thin oxide layer acts as an active resistive switching layer when electrically contacted. Indeed Cagli et al. demonstrate that two crossed nanowires may be operated as a resistive switch, as the nanowire junction naturally creates a metal-oxide-metal structure.[12] The effect of incorporating a resistive switching element into a nanowire network is investigated in chapter 5. Prior to this however, the junction resistance and resistive switching properties of single junctions are first established.

This chapter begins by describing the synthesis methods used to make both Ag and Ni nanowires, then the methods used to fabricate single junctions will be described. Following this the electrical characterisation of single junctions will be described, and the junction resistance measured for each system. The chapter concludes by examining Ni nanowire junctions using impedance spectroscopy.

3.2 SINGLE NANOWIRE JUNCTION FABRICATION

3.2.1 NANOWIRE FABRICATION & PREPARATION

3.2.1.1 Ag Nanowires

Ag nanowires were purchased from Seashell Technology,[13] dispersed in isopropyl alcohol (IPA). Prior to use, the as-received solution is diluted to an approximate concentration of 0.1 mg/ml. The nanowires are fabricated through the polymer-mediated polyol process.[14,15] $AgNO_3$ is reduced by ethylene glycol in the presence of poly(vinyl pyrrolidone) (PVP). At a critical concentration of elemental Ag, metallic clusters begin to nucleate. These clusters may then continue to grow to form nanostructures in a variety of shapes. The growth of nanowires is made favourable by limiting the $AgNO_3$ and PVP concentrations, lowering the chemical potential for growth such that the thermodynamically favourable multiply-twinned decahedra form, rather than the kinetically favoured single-crystal seeds. These elongate as further growth occurs on the {111} face. PVP acts as a capping agent, interacting more strongly with the {100} face, and further facilitating the growth of the {111} face and the elongation of the wire. Figure 3.1 shows SEM and TEM images of the nanowires, clearly displaying pentagonal twinning. As a result of this fabrication process, each nanowire is coated in a thin (2–5 nm) layer of PVP, highlighted in the TEM images shown in Figure 3.1. Length and diameter statistics, generated using both SEM and AFM, are also shown. The nanowires have an average length of $7.3 \pm 3.4 \, \mu m$, and an average diameter of $85.7 \pm 17.6 \, nm$.
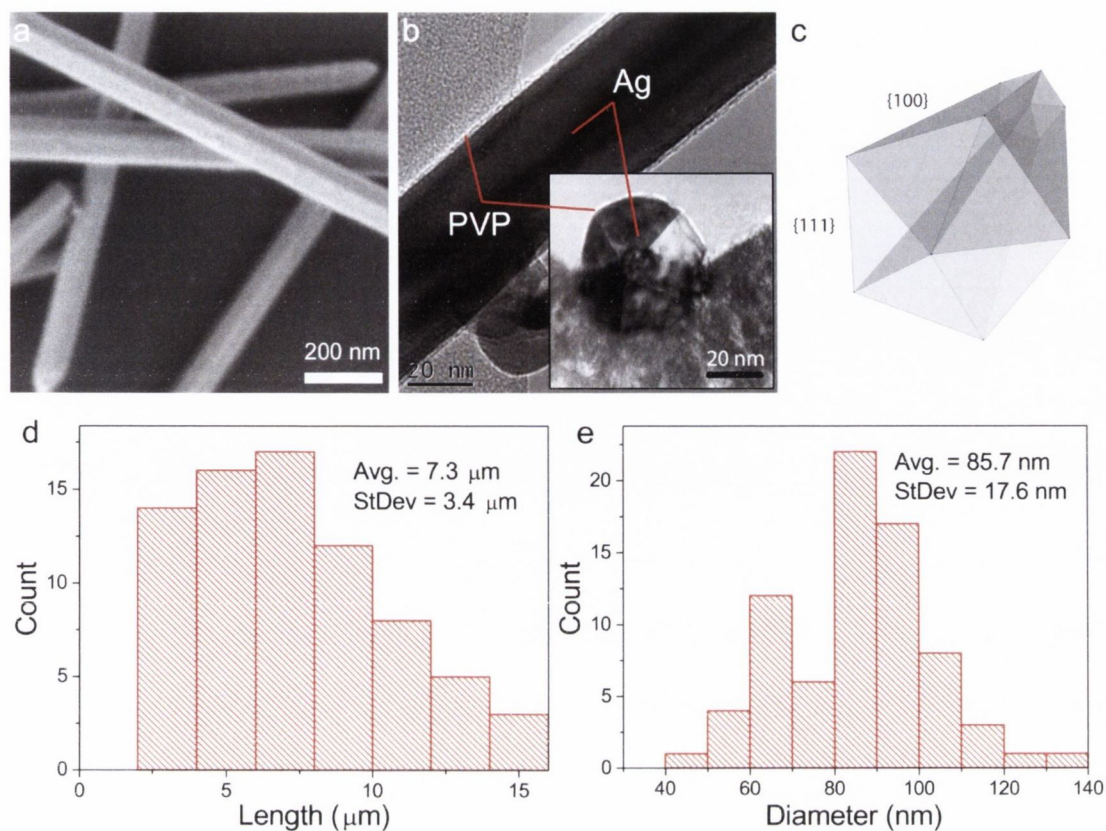
FIGURE 3.1. Characterisation of PVP-coated, pentagonally twinned Ag nanowires. (a) SEM image of Ag nanowires. (b) High resolution TEM image of a nanowire, clearing showing the PVP surface coating. Inset shows a TEM cross-section image of a nanowire, displaying the pentagonally twinned nature. (c) Illustration of the different crystallographic faces of a Ag nanowire. (d) and (e) show the length and diameter statistics, respectively, of the Ag nanowires used in this work.

3.2.1.2 Ni Nanowires

Ni nanowires were purchased from Nanomaterials.it.[16] The nanowires are synthesised by electrodeposition into nanoporous anodised aluminium oxide (AAO) templates, and are received as-fabricated in these templates. The nanowires were removed from the template through the following extraction procedure. The Au backing electrode was removed using *aqua regia* (HNO_3:HCl 1:3 vol) and a cotton swab. The AAO template was then washed in deionised (DI) H_2O, and placed in a 0.1 M NaOH solution until the template dissolved ($\sim$ 4 hours). Mild sonication was used to help break up the template and accelerate the dissolution process. Once dissolved, the nanowires were separated from the NaOH using a magnet to collect the nanowires together while the solution was decanted off. The nanowires were then washed with DI H_2O three times to remove any remaining NaOH, then washed with HPLC grade IPA three times. Between each wash step the dispersion was centrifuged at 4500 rpm for 5 minutes to draw the nanowires to the bottom of the vial so that the supernatant could be decanted off. Finally a stock solution was prepared by dispersing the

nanowires in HPLC IPA at a concentration of approximately 2 mg/ml.

For consistency, and unless otherwise stated, all results presented in this thesis are from the same batch of nanowires, labelled NB5. The nanowires were characterised by SEM, HIM, TEM and EDX, a sample of which are shown in Figure 3.2. SEM and AFM were used to develop length and diameter statistics, while TEM analysis, performed by Dr Eoin McCarthy, was used to develop statistics on the oxide thickness. The nanowires are polycrystalline in nature, as shown in Figure 3.2(b). The nanowires have an average length of $10.6 \pm 6.7\,\mu$m, an average diameter of 81.3 ± 6.9 nm, and an average oxide coating of thickness 6.0 ± 1.4 nm.

3.2.2 JUNCTION FABRICATION & CONTACTING

As mentioned in chapter 2, the fabrication of contacts to individual nanoscale objects requires a combination of UV lithography and EBL. In order to obtain isolated crossed nanowires, Si wafers patterned using UV lithography (see Figure 2.13 for mask design), were cleaved into individual 6×6 device arrays – approximately 25 mm^2 in area. Extremely dilute dispersions were made from the stock nanowire solution ($\sim 12\,\mu$g L^{-1}), and then a very small volume ($\sim 20\,\mu$L) of this was dropped onto each individual sample and allowed to evaporate in a fume hood. This was repeated multiple times until a sufficient number of isolated crossed junctions had been formed. TEM measurements of Ag nanowires that have undergone similar steps show no change in the PVP coating following this processing.

In the case of the magnetic Ni nanowires, this process was aided by placing each sample on a bar magnet such that the field lines ran parallel with the axes defined on the sample. Once the solvent has evaporated, the nanowires lie aligned in the direction of the field. The sample is then rotated 90°, and the step repeated. This magnetic alignment procedure aided the formation of perpendicular crossed nanowires, and has been previously reported by Cagli et al.[12] Once located, contacts were then formed onto the junctions using EBL and metal evaporation, as outlined in chapter 2. To ensure complete coverage of the metal, the thickness of the evaporated layer was set to be approximately twice the diameter of the nanowire – 150 nm in most cases. In almost all cases, Ag nanowires were contacted with Ag metal lines in order to minimise the contact resistance. Similarly, Ni nanowires were contacted almost exclusively with Ni metal. Figure 3.3 shows an example of a contacted nanowire junction, showing the progression in feature size from the UV lithographic mask to the EBL defined fingers, and finally shows a high magnification image of the junction. To enable 4-probe measurements across individual junctions, two metal contacts were formed on each nanowire that made up the junction, as can be seen in Figure 3.3(b).
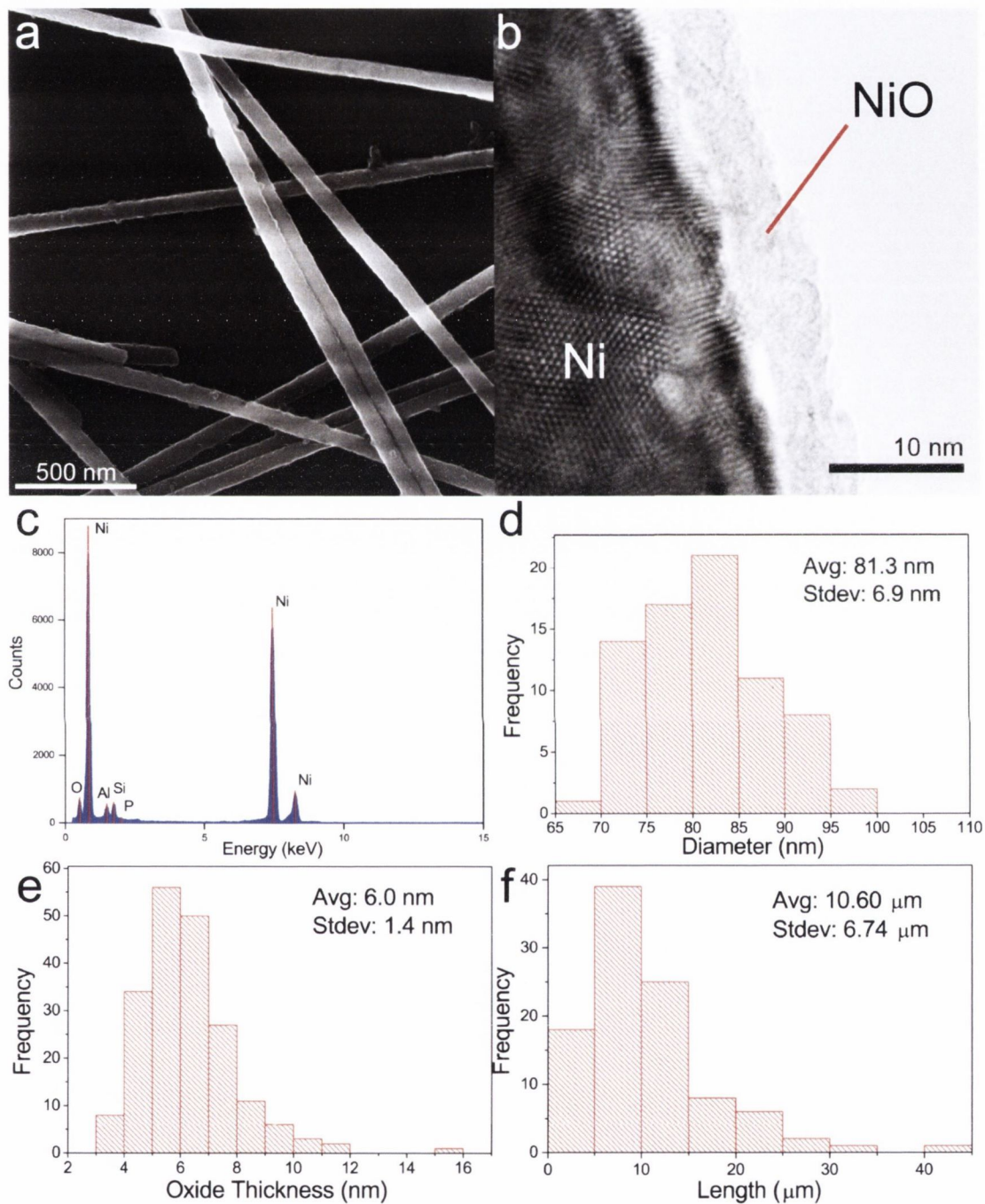
FIGURE 3.2. Characterisation of extracted Ni nanowires. (a) SE image of Ni nanowires produced in a HIM. (b) High resolution TEM image of a Ni nanowire, showing the polycrystalline nature of the Ni core as well as the amorphous NiO surface coating. (c) EDX analysis performed on a single Ni nanowire in a TEM. (d), (e), and (f) show diameter, oxide thickness, and length statistics respectively of the Ni nanowires from batch NB5.
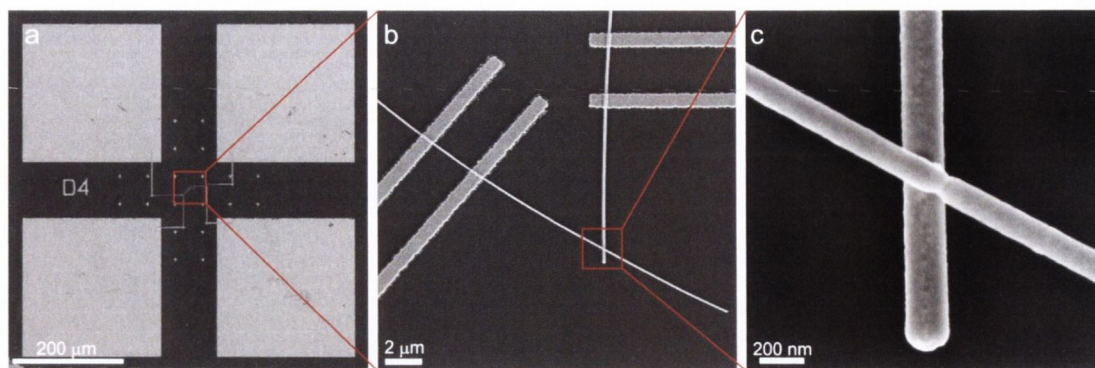
FIGURE 3.3. SEM images of a single Ag nanowire junction with four Ag metal contacts fabricated with EBL.

3.3 DC ELECTRICAL MEASUREMENTS: RESISTIVE SWITCHING & R_{jxn}

The motivation behind performing measurements on single nanowire junctions has been described, as have the methods used to fabricate and contact these nanoscale structures. The following section will detail the results of the DC electrical measurements on both Ag and Ni nanowire junctions.

3.3.1 Ag NANOWIRE JUNCTIONS

3.3.1.1 Annealed Nanowires

As explained in section 3.2.1, Ag nanowires fabricated through the polyol process are produced with a thin PVP coating on the surface of the nanowire. In order to ensure ohmic contact between the nanowire and the Ag metal contact lines, this PVP layer must be removed. This is performed by annealing the sample in a tube furnace under N_2 flow, prior to contacting. The wires are heated to 200 °C for 2 hours. Ag nanowire networks fabricated for transparent conductor applications are routinely subjected to a heat treatment step to reduce the junction resistance and increase the conductivity of the network,[1,5,7] and this step is consistent with this.

Prior to measuring on single junctions, initial measurements were performed on individual Ag nanowires in order to determine the resistivity for the subsequent calculations of nanowire resistance. Figure 3.4(a) shows an AFM image of a single Ag nanowire contacted with four electrodes for 4-probe measurement of the resistance. The resistivity of the nanowire was calculated using equation (2.4), where L was measured from the outside edges of the inner electrodes, as per Kolesnik et al.,[17] and shown in the figure. The diameter was measured from AFM analysis at different points along the nanowire, and an average value obtained. The results are plotted in Figure 3.4(b) for the five nanowires measured, where the diameter of the nanowires was in the range 74–86 nm. The average resistivity
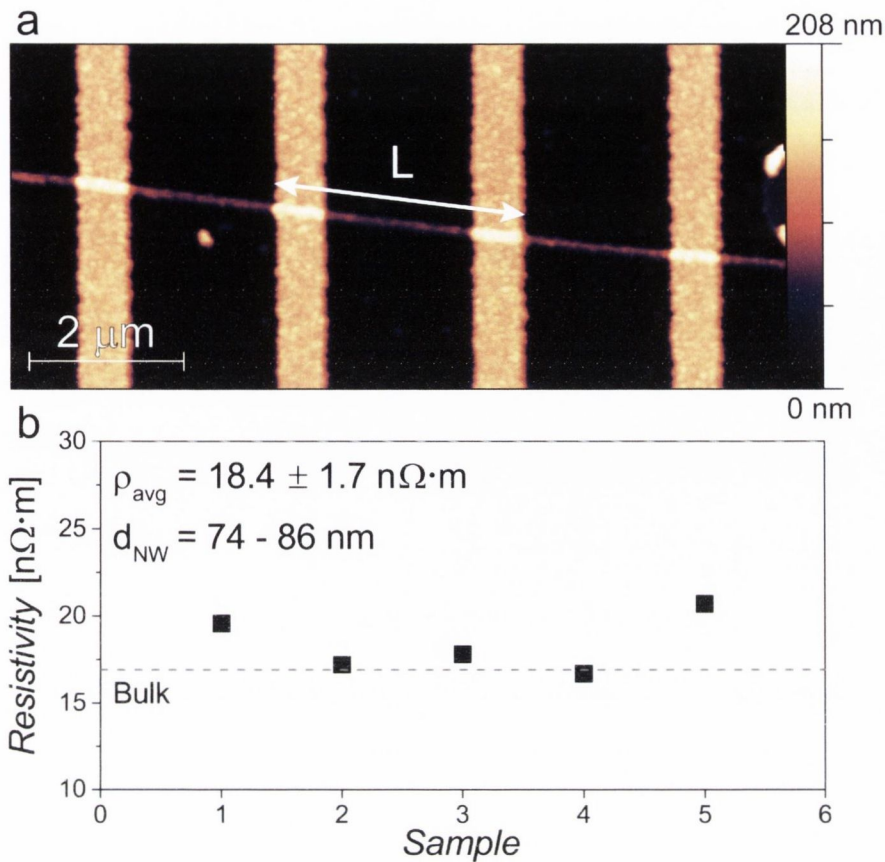
FIGURE 3.4. Resistivity measurements of single Ag nanowires. (a) AFM topography image of a single Ag nanowire contacted with four Ag electrodes for measurement of the resistivity. (b) Measured resistivity of five different nanowires, with diameters in the range 74–86 nm. An average resistivity value of $18.4 \pm 1.7 \, \text{n}\Omega \cdot \text{m}$ was determined.

was found to be $18.4 \pm 1.7 \, \text{n}\Omega \cdot \text{m}$, within experimental error of that of bulk Ag – $15.9 \, \text{n}\Omega \cdot \text{m}$. Kolesnik et al. also show no deviation from the bulk resistivity for similar multiply-twinned Ag nanowires, consistent with this result. The resistivity of the nanowires was then taken to be equal to that of bulk Ag, and this value was used to calculate the resistance of a length of nanowire in subsequent measurements of R_{jxn}.

Following the establishment of a nanowire resistivity, the junction resistance was then measured. By performing a 4-probe measurement across the junction, the 2-probe resistance of the outer circuit, R_{out}, as well as the 4-probe resistance of the inner circuit, R_{in}, are produced – as depicted in Figure 3.5. Contained within R_{in} are the resistances of the nanowire lengths ($R1$ and $R2$ respectively) and the junction resistance, R_{jxn}. By measuring the distance between the electrode and the junction for each nanowire ($L1$ and $L2$, respectively), the average diameter of each nanowire ($d1$ and $d2$, respectively), and using the resistivity of bulk Ag the resistance contributions from $R1$ and $R2$ may be accounted for. The junction resistance is then isolated through the calculation $R_{jxn} = R_{in} - R1 - R2$.

The calculated values of R_{jxn} are tabulated in table 3.2 alongside the measured resis-
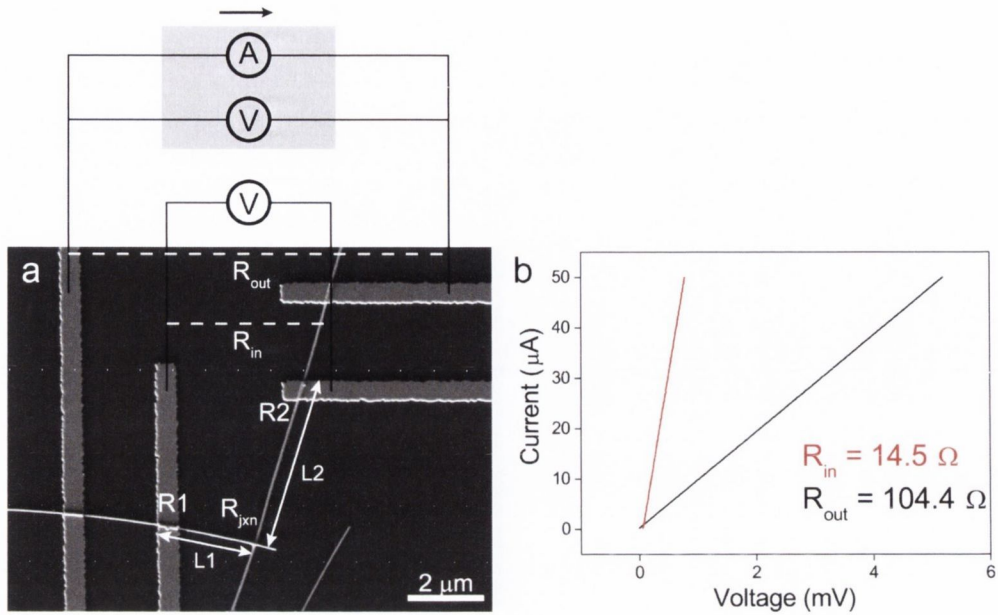
FIGURE 3.5. Junction resistance experimental set-up. 4-probe measurement is performed, sensing voltage across inner electrodes. The measured resistance is then the sum of three resistances: R1, R2, and R_{jxn}. R1 and R2 may be calculated and removed from the measured resistance, providing accurate measurement of R_{jxn}.

tances, R_{out} and R_{in}, and the contact resistance, R_{cont}, where $R_{cont} = R_{out} - R_{in}$. Immediately apparent is the range of values obtained, ranging from very small values of only a few ohms to hundreds of ohms. The majority of the values calculated however are below 50 Ω, indicating that the values measured to date have significantly overestimated the junction resistance. It is also apparent from this table that the contact resistance remains very uniform for almost all samples measured, indicating the same measurement environment throughout and strengthening the results.

In order to further understand the results presented in table 3.2, all measured junctions were characterised with SEM. Figure 3.6 shows the SEM images for nine of the junctions listed in table 3.2. The R_{jxn} corresponding to each junction is included alongside each image, which are arranged in order of increasing R_{jxn} from left to right. Of particular interest is panel (c), as it displays a clear melting, or "welding" of the junction between the two wires, which is likely a result of the 200 °C annealing step. Panels (a), (e), (f), and (g) also display similar features indicating localised welding of the junction, though not quite as apparent as in (b). Similar junction welding has been reported by others, notably Garnett et al. in 2012, and Song et al. in 2014.[8,9] In both cases, welding of the junction is demonstrated to be the result of treatment by plasmonic excitation and thermal annealing respectively, however neither group report R_{jxn} values as low as those measured here, which are an order of magnitude smaller than the lowest previously reported measurement. It is interesting to note that even junctions displaying this localised welding still have an appreciable R_{jxn}, as high as 51 Ω for the junction in panel (g). Conversely, junctions displaying no such welding

TABLE 3.2. Measured and calculated resistances from 4-probe measurements of single Ag nanowire junctions. R_{out} and R_{in} are the 2-probe and 4-probe measured resistances produced from the measurement, and R_{cont} is the contact resistance. R_{jxn} and ΔR_{jxn} are the junction resistance and calculated error respectively. The corresponding panels in Figure 3.6 are indicated in square brackets.

Sample		R_{out} (Ω)	R_{in} (Ω)	R_{cont}	R_{jxn} (Ω)	ΔR_{jxn} (Ω)	Activation
A120-04;F4	[a]	104.4	14.5	89.9	3.8	0.5	anneal
A120-06;C2	[b]	100	26.7	73.3	6	1	anneal
A120-04;A1	[c]	521	27.5	493.5	8	1	anneal
A120-06;C6	[d]	84.1	31.6	52.5	10	1	anneal
A120-04;F1		112.3	51.6	60.7	12	1	anneal
A120-04;C2T	[e]	131.3	51.2	80.1	20	2	anneal
A80-01;D5	[f]	443	44	399	25	1	anneal
A120-04;B6	[g]	191.3	96.3	95	51	5	anneal
A120-04;F1T	[h]	300.8	74.5	74.5	93	4	anneal
A120-06;E2	[i]	387.7	309.6	78.1	242	3	anneal

features may show very low resistances, such as that in panel (b) where R_{jxn} is only 6 Ω.

This result may indicate the presence of contaminant materials at the junction. To examine the composition of the junctions, EDX analysis was performed in the SEM chamber. The results of this analysis are shown in Figure 3.7 for the junction in Figure 3.6(c). At an accelerating voltage of 20 kV only Si, O, and Ag peaks appear in the EDX spectrum. As both Si and O peaks are expected due to the 300 nm SiO$_2$ substrate, it may be concluded that the junction contains no metallic impurities, however hydrocarbon contaminants may still be present. A similar analysis was performed for the other junctions measured, and in all cases no heavy element contaminant material was detected.

The results presented above for the case of annealed wires present a clear picture regarding the state of the junctions within a network. The values obtained have a distribution spanning hundreds of ohms, with the majority of values lying below 50 Ω. Comparing these values to those previously measured, as well as those that have been estimated from combined experiment/simulation results, it is clear that in the literature to date there has been an overestimation of the true junction resistance. The implication of this result is that future simulations performed on random nanowire networks must account not only for the junction resistance, but also for the intra-wire resistance. To date this has generally been ignored (with the exception of Hu et al.), assuming a much larger contribution from the junction. These results show however that the resistance of the junction and that of the nanowire are of the same order of magnitude, and thus both must be accounted for if the
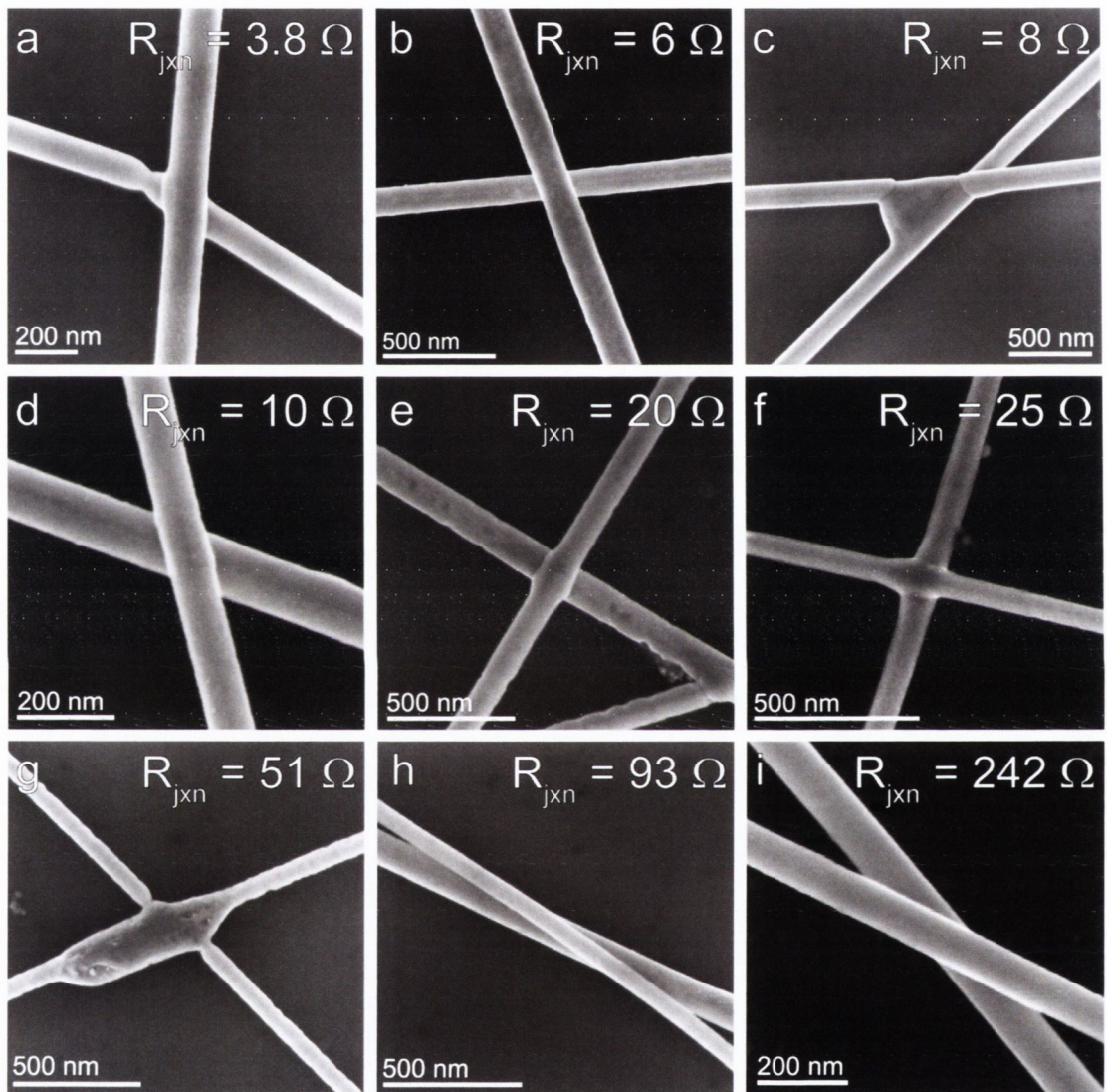
FIGURE 3.6. SEM images of annealed Ag nanowire junctions. The images are arranged with increasing R_{jxn} going from left to right. It is clear that a range of different junction morphologies are obtained following the annealing step. Panels a, c, e, f, and g, are noteworthy as they appear to display "welding" at the junction.
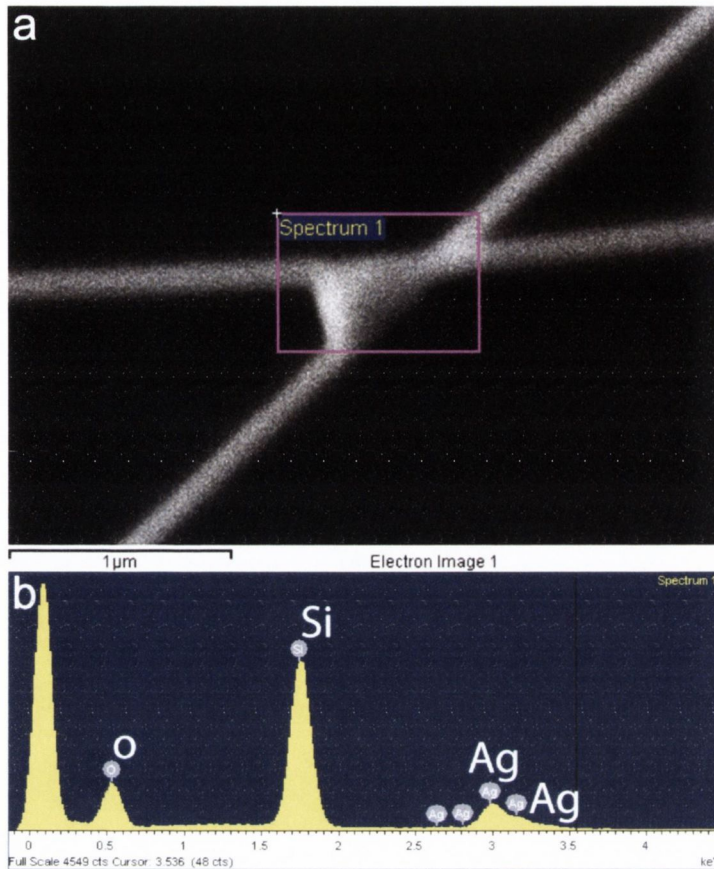
FIGURE 3.7. EDX analysis of welded Ag nanowire junction. Scan was performed on highlighted area, at an accelerating voltage of 20 kV. Apart from Ag, only Si and O peaks from the substrate are present, indicating no heavy element contamination of the junction.

model is to be accurate.

Additionally, the simulation results obtained by Hu et al. are validated in the context of these new findings. In order to fit the experimental data to their simulations, a range of values of R_{jxn} values were used, namely 1, 40 and 100 Ω. This range of values maps well onto the values measured directly in this work. Therefore at higher network densities, there will be enough nanowires to connect the lower resistance junctions, thereby shifting the total sheet resistance to lower values. This highlights the importance of understanding the distribution of R_{jxn} values present in a network in order to understand the effect of network density on the resistance of the film.

3.3.1.2 Electrically Activated Junctions

The results of the junction resistance obtained for annealed wires are extremely significant in the context of understanding the contributions to the sheet resistance from the junctions. This also brings into play a question regarding how much of an effect the annealing process has on the low junction resistances measured. Furthermore, what effect does the PVP have on the conduction properties of non-annealed nanowires, and can this be affected
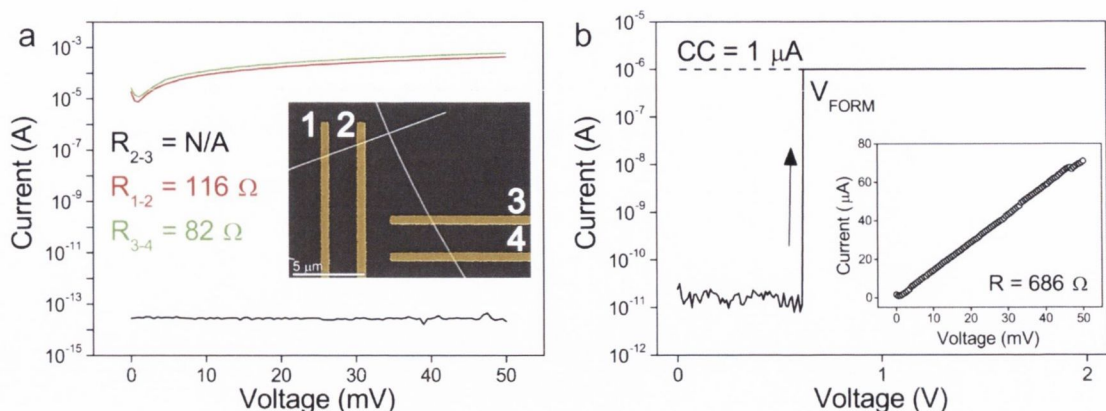
FIGURE 3.8. I-V curves of a non-annealed Ag nanowire junction. (a) Initial low bias sweeps across three electrode pairs: 1-2, 3-4, and 2-3 (junction). Adjacent electrodes (1-2, and 3-4) show ohmic behaviour and very low resistances of $\sim 100\,\Omega$, while the junction is highly insulating and only noise is measured. (b) Sweeping 2 V across electrodes 2-3, the current suddenly jumps to a pre-defined compliance current of $1\,\mu A$ at 620 mV. Inset shows subsequent low bias I-V sweep showing a resistance of $686\,\Omega$.

through electrical stressing? This section focuses on measuring the junction resistance of non-annealed Ag nanowire junctions.

For the work presented in this section, Ag nanowire junctions were prepared using the same method as described in section 3.2.2, however the annealing step was omitted to prevent the removal of the PVP layer at the junction. To begin, a low bias sweep was performed across each pair of electrodes contacting each nanowire. It was found that in the majority of cases there was an ohmic connection between the electrodes, showing a low resistance of $\sim 100\,\Omega$ – shown in Figure 3.8(a) as the red and green trace respectively. This indicates the possible breakdown of the PVP layer during the contacting procedure – likely occurring during deposition of the contact metal. The same low bias sweep was applied across the junction (electrodes 2 and 3) as shown by the black trace in Figure 3.8(a). It was found that no detectable current flowed through the junction, even at the highest current sensitivities.

The PVP passivation layer therefore prevents the flow of current through the junction at low bias. To measure the limits of this conduction barrier, a larger voltage sweep was applied across the junction. Figure 3.8(b) shows the I-V behaviour as the voltage is swept to 2 V. It can be seen that initially no current is detected, measuring at the noise limits of the instrumentation. However at a voltage of 620 mV, a sudden jump in the current is seen, rising by five orders of magnitude to hit the pre-defined compliance current (CC) of $1\,\mu A$. Following this, another low bias sweep was performed, shown inset in Figure 3.8(b). The 2-probe resistance of the junction had now decreased to $686\,\Omega$. A subsequent 4-probe measurement produced an R_{jxn} value of $475\,\Omega$.

As this value was high in comparison to values measured for annealed junctions, current was driven through the junction in an attempt to lower the resistance by strengthening the
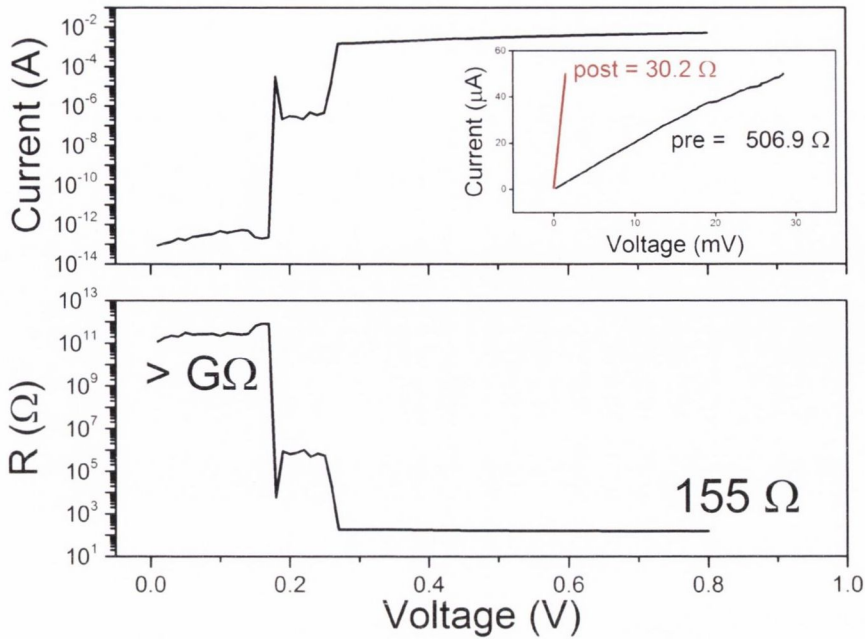
FIGURE 3.9. Current driven strengthening of a Ag nanowire junction. The current-voltage and resistance-voltage plots shows an initially very high resistance (> GΩ) of the junction, but this quickly reduces as the voltage is swept, reaching a plateau of 155 Ω. Inset: 4-probe measurements made before and after show a decrease in R_{in} of 477 Ω. It is suspected this reduction in the junction resistance is a current driven process.

connection between the nanowires. It is well established in the field of resistive switching, that current has a significant effect on the resistance of the conductive filament.[18,19] The same logic is applied here. Figure 3.9 shows the current and resistance response of the junction as the voltage is swept to 1 V across electrodes 2-3 with no current compliance set. At the beginning of the voltage sweep, the resistance is approximately 0.1 TΩ – this is contrary to the previous figure which demonstrated a resistance of 686 Ω. The reason for this extreme jump in resistance is unknown. However, the resistance of the junction quickly drops at 180 mV, and continues to decrease until a plateau is reached at 155 Ω. Following this procedure, the 4-probe measurement was repeated and a new R_{in} value of 30.2 Ω was observed – Figure 3.9, inset. The total resistance contributed by the nanowires was calculated to be 32 ± 2 Ω, resulting in a junction resistance of −2 ± 2 Ω, or an effectively zero contribution to the measured resistance.

The electroforming process described above demonstrates that it is possible to create a highly conductive nanowire junction without the use of a thermal annealing step. The behaviour itself shows many similarities to that of resistive switching, as the junction exhibits two resistance states which may be switched between under the action of an electric field, while the choice of compliance current affects the strength of the LRS. For the Ag/PVP/Ag junction however, the process is irreversible, and it is suspected that the PVP at the junction is permanently modified due to the Joule heating that results from the extreme current densities. In the following section, the electrical properties of resistive switching Ni/NiO/Ni

TABLE 3.3. Measured resistance values and the calculated R_{jxn} for electrically activated nanowire junctions. The corresponding panels in Figure 3.10 are indicated in square brackets.

Sample		R_{out} (Ω)	R_{in} (Ω)	R_{cont}	R_{jxn} (Ω)	ΔR_{jxn} (Ω)	Activation
A120-05;D2	[a]	113.2	30.2	83	-2	2	electroform
A120-05;D4	[b]	100.5	40.7	59.8	23	1	electroform
A120-01;E3	[c]	164	97	67	31	3	electroform
A120-01;C6	[d]	217	124	93	58	6	electroform
A120-02;A2	[e]	1034	328	706	292	3	electroform

nanowire junctions will be discussed, where the system is known to be reversible.

The above electroforming procedure was followed for a number of different Ag nanowire junctions, with each showing a similar behaviour, the results of which are tabulated in table 3.3. For the five junctions measured, all show reasonably low R_{jxn} values, below $60\,\Omega$, with one exception showing a particularly high value of $292\,\Omega$. The measured contact resistance for this sample was also extremely high ($706\,\Omega$), so it is likely that the measurement conditions were not ideal, possibly resulting in an artificially high R_{jxn}. SEM characterisation of each junction was performed, and is shown in Figure 3.10.

The images reveal a number of interesting properties about the junctions. Firstly, unlike the annealed nanowire junctions, no evidence of junction welding is present, despite being subjected to high current densities. This indicates then that it is the thermal treatment step that is the cause of the "welding" features observed previously. This also indicates that welded junctions are not required in order to achieve very low junction resistances. This is a particularly important result for the work presented in chapter 4. In panels (c) and (d) in Figure 3.10, there is evidence of folding of the top nanowire around the underlying one. This would increase the contact area between the nanowires, and aid in producing a low junction resistance, however only thinner nanowires are malleable enough to display this behaviour.

Finally, the results obtained for both annealed and electroformed Ag nanowire junctions were combined, and are shown in Figure 3.11 as a histogram. While many more data points are required to determine the exact form of the distribution, the data collected thus far resembles a highly skewed normal distribution. The mean of the distribution was calculated to be $58\,\Omega$ while the median value is $23\,\Omega$. It is clear then, based on the evidence presented thus far, that the junction resistance is significantly smaller than previously suggested, implying that both junction resistance and resistance of the nanowire must be equally accounted for when simulating random networks composed of these materials.
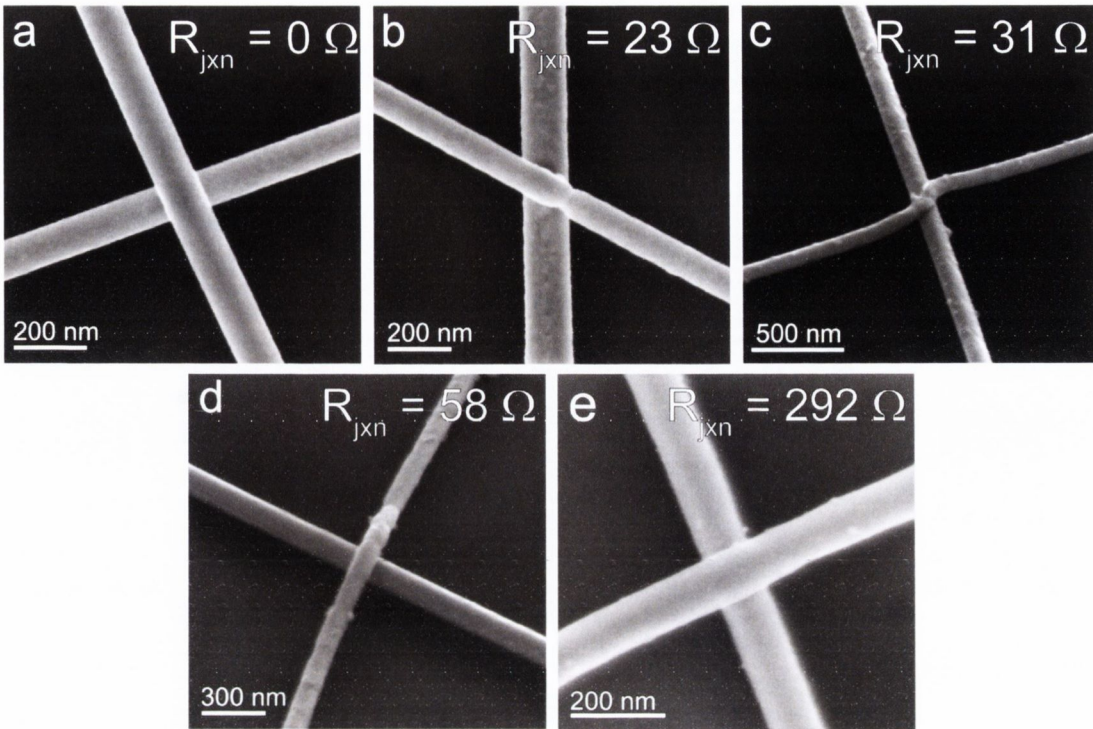
FIGURE 3.10. SEM characterisation of electroformed Ag nanowire junctions. Unlike for the annealed nanowires, evidence of junction welding is not apparent, yet low junction resistances are still obtained. In the case of the junction in panel (a), no measurable R$_{jxn}$ value was obtained. It is also not clear, based on this evidence, why the junction in panel (e) displays a value almost 250 Ω larger than all other junctions shown.
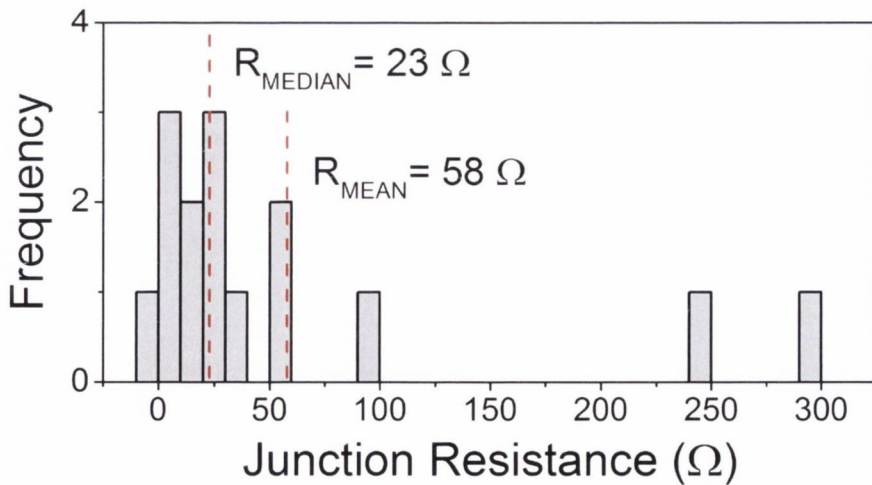
FIGURE 3.11. Histogram of all R$_{jxn}$ values measured for Ag nanowires. The mean and median values are indicated by red dashed vertical lines, and the corresponding values are shown in each case.

3.3.2 Ni Nanowire Junctions

As mentioned at the beginning of this chapter, there are various reasons to study the junction properties of nanowires made of materials other than Ag, and Ni presents an interesting alternative. The presence of a native, passivating oxide on the surface of Ni nanowires presents some technologically relevant opportunities, such as oxidation resistant, flexible, transparent conductors, but also poses challenges as the nanowire cores are initially electrically isolated and thus must be connected. In this section, the electrical properties of Ni nanowire junctions are investigated.

To begin, single nanowires of Ni were electrically contacted using the methods described previously, where Ni was chosen as the contact metal in all cases and no annealing step was performed on these wires. As shown in Figure 3.2, the nanowires have a native NiO surface coating, an average of 6 nm in thickness. The history and mechanism of NiO as a resistive switching material was described in detail in chapter 1, but will be summarised again here for clarity. Application of an electric field across a nanoscale NiO film induces the formation of a conductive Ni filament which at a voltage, V_{FORM}, spans the width of the insulating oxide and creates a low resistance pathway for current to flow, known as the low resistance state (LRS). By then driving sufficient current through the nanoscale filaments, Joule heating causes the partial dissolution of the filament into the surrounding NiO matrix at a current, I_{RESET}, and the high resistance state (HRS) is generated. Reapplication of a sufficient voltage may regenerate the LRS as the filaments are reformed, though the voltage required, V_{SET}, is lower than that required during the initial forming.

Therefore, in order to establish an ohmic contact between the contacting metal and the underlying Ni core, a voltage was swept across two adjacent electrodes on a single nanowire until the sudden decrease in resistance was observed. This is illustrated in the I-V plot shown in Figure 3.12. A compliance current (CC) is set during each forming or set event in order to limit the current passing through the nanowire and prevent a catastrophic failure of the nanostructure. During the initial forming, the CC was sequentially increased from 100 nA to 1 μA to 10 μA. It was found that nanowires have a tendency to fail if the initial CC is too large, hence this sequence of forming steps. Once a stable filament had formed, sequential forming was omitted for subsequent cycles, and instead the CC was set to 10 μA.

For the lower values of CC the resistance state is not retained – a behaviour known as threshold switching – however it is clear from Figure 3.12 that the slopes of each sweep are different, indicating that a physical change has occurred. It is not until a current level of 10 μA is reached that the state is retained at zero bias, demonstrating non-volatile switching. This is in contrast to the behaviour witnessed by He et al. on single Ni/NiO core-shell nanowires, where a CC value of 100 μA was required to establish memory switching.[20]

Also included in Figure 3.12 is an equivalent circuit model for a single Ni nanowire contacted by four electrodes in a 4-probe measurement scheme. Each contact has been represented as a switch as each creates an MIM structure, and is therefore capable of
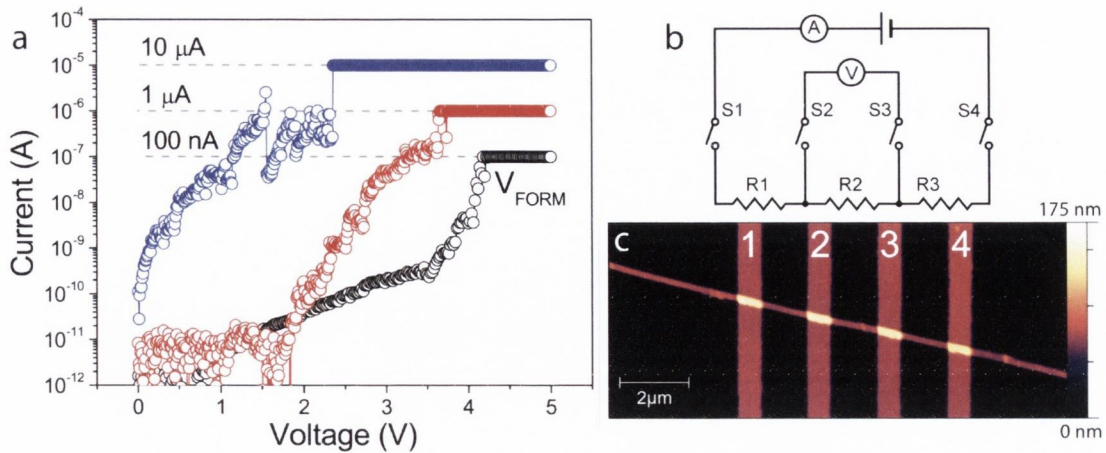
FIGURE 3.12. Electroforming and ohmic contact formation on a single Ni nanowire. (a) I-V curves show the forming process used to generate an ohmic contact between Ni contact metal and a single Ni/NiO core-shell nanowire (AFM image of which is shown in (c)). The value of CC is increased step-wise until memory switching is achieved. (b) The equivalent circuit of a 4-probe measurement on a pristine Ni nanowire, illustrating the possible switching locations.

resistively switching. Once each electrode pair had been formed fully, the resistivity of the nanowire could then be measured. As in the case of Ag nanowires, it is important to verify the resistivity of the nanowires prior to any measurement of the junction resistance. Accurate length and diameter measurements of the nanowire were made and the resistivity calculated from the 4-probe resistance measured between electrodes 2 and 3 (Figure 3.12(c)). While calculating the radius of the nanowires, the presence of the passivating oxide must be taken into account. As the true value of t_{ox} for each nanowire could not be measured, an average value was used, and so there is a higher degree of uncertainty in the final value of ρ_{NiNW} obtained. Due to the difficulty of the measurement, the resistivity of only three nanowires was obtained, the average value of which was $62 \pm 19 \, \text{n}\Omega \cdot \text{m}$. Compared to the resistivity of bulk Ni, $69.3 \, \text{n}\Omega \cdot \text{m}$, this result is within the limits of experimental error, and the resistivity of the nanowire was therefore deemed not to deviate from that of the bulk.

Once the nanowire resistivity was established, the junction resistance of Ni nanowires was then investigated. Unlike Ag nanowires however, which may be annealed to create an ohmic contact, the Ni nanowire junction is always highly resistive in the pristine state and thus must be switched to a LRS before measurement of R_{jxn} can be made. The measurement is further complicated by the fact that each contact-nanowire interface must also be switched to a LRS prior to measurement. A strict measurement protocol must then be followed, where each "leg" of the junction is switched independently, following the same procedure as outlined above for the single Ni nanowire measurements, after which the junction may be addressed. This measurement protocol is summarised below, where the electrodes labelled 1–4 correspond to those labelled in Figure 3.13(a).
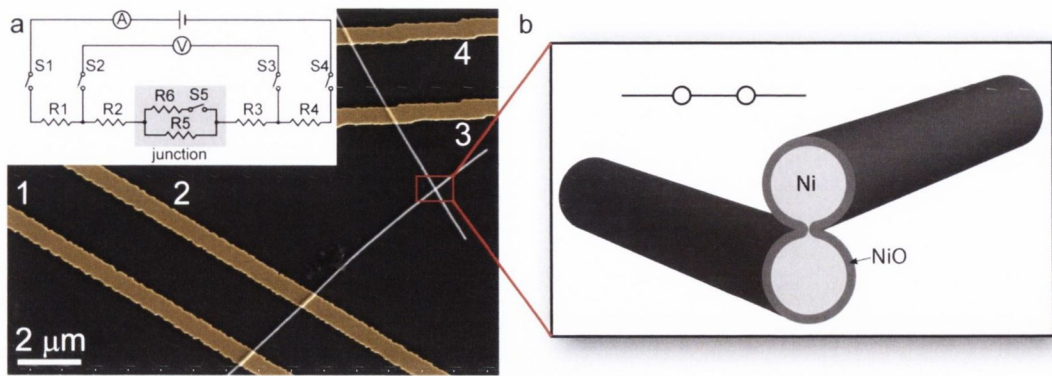
FIGURE 3.13. 4-probe measurement of R_{jxn} in Ni nanowires. (a) False-colour SEM image of Ni nanowire junction contacted with four electrodes for 4-probe measurement. Prior to measuring the junction, each electrode pair (1-2, and 3-4) must be formed to the LRS. Inset: Equivalent circuit of the 4-probe measurement. (b) Schematic of the junction in the LRS, where a thin metallic filament percolates through the insulating NiO layer.

Protocol for the measurement of R_{jxn} in Ni nanowires.

1. Form electrode pair 1-2 to 10 µA.

2. Verify LRS of 1-2 by performing low-bias sweep. Values below 5 kΩ are typical.

3. Form electrode pair 3-4 to 10 µA. Verify LRS with low-bias sweep.

4. Perform low-bias sweep across junction (electrodes 2-3).

5. Sequentially form junction to 100 nA, 1 µA, and 10 µA.

6. Perform low-bias sweep after each forming step. Verify establishment of LRS post 10 µA forming step.

7. Perform 4-probe measurement across junction, sourcing across electrodes 1-4 and sensing across electrodes 2-3.

Figure 3.13 shows an SEM image of a contacted Ni nanowire junction, with the metal contacts false coloured for clarity. Also shown is the equivalent circuit for this measurement, where each contact-nanowire interface is represented as a switch, and the junction itself is considered as a parallel circuit of two resistors and a switch. A schematic of the junction cross-section is shown in Figure 3.13(b), where the junction is depicted as being in the LRS. Direct observation of a conductive filament in a nanoscale junction such as this is extremely challenging, however based on the observations of conductive filaments in TiO_2 made by others,[21] it is suspected that the filaments formed through the junction are only a few nanometers in diameter. It is therefore expected that the junction resistance for

TABLE 3.4. Measured and calculated resistance values of Ni nanowire junctions. The corresponding panels in Figure 3.14 are indicated in square brackets.

Sample		R_{out} (Ω)	R_{in} (Ω)	R_{cont}	R_{jxn} (Ω)	ΔR_{jxn}
NB5-30;C2	[a]	1538	327	1211	**194**	44
		1759	557	1202	**423**	45
		2226	1025	1202	**892**	45
NB5-25;A1	[b]	3151	459	2692	**305**	44
		6060	800	5260	**647**	44
NB5-20;D1	[c]	3210	929	2281	**435**	172
NB5-27;A3	[d]	3434	1395	2039	**908**	187
NB5-20;D1T	[e]	3290	1260	2030	**1110**	44
NB5-20;B3	[f]	3680	1740	1940	**1550**	56

Ni nanowires will be considerably larger than that measured for Ag nanowires, which are expected to have a contact area of the order 40×40 nm^2, based on their pentagonal geometry.

Table 3.4 shows the R_{jxn} measurements obtained on six separate junctions, including also the R_{out} and R_{in} values as well as the calculated contact resistance. It is apparent from this table that the junction resistance for Ni is indeed considerably larger than that of Ag, having an average value of 718 Ω, with a standard deviation of 437 Ω. Such a large value is to be expected, given the nanoscale filament size and the higher resistivity of bulk Ni. Indeed, it may be possible that the filament is sufficiently small so as to introduce electronic confinement effects, thereby making the use of the bulk resistivity inappropriate in this context. However, values of 194 Ω were also measured, indicating that relatively low junction resistances are possible, despite the nanoscale nature of the junction. Also apparent from table 3.4 is the very large values obtained for R_{cont}, the contact resistance, as values as large as 5.2 kΩ were calculated. This is likely a result of the thin ohmic contact formed between the metal contact lines and the Ni nanowire. The measured values of R_{jxn} show values considerably larger than a similar measurement made by Cagli et al., discussed in chapter 1.[12] They measure a 2-probe resistance of 265 Ω across an activated Ni/NiO core-shell nanowire junction. Despite not accounting for the contact resistance in the measurement, this value is still close to the lowest values measured in this study. The reason for the discrepancy in these junction resistance values is not clear. It should be noted that unlike Ag nanowire junctions, current-induced enhancement of the resistance was not observed in Ni nanowires, as the junctions switch to a HRS at moderate to high current densities.

For two of the six samples shown in table 3.4, multiple values of R_{jxn} are presented. For these samples, the resistance state of the device was cycled a number of times to investigate
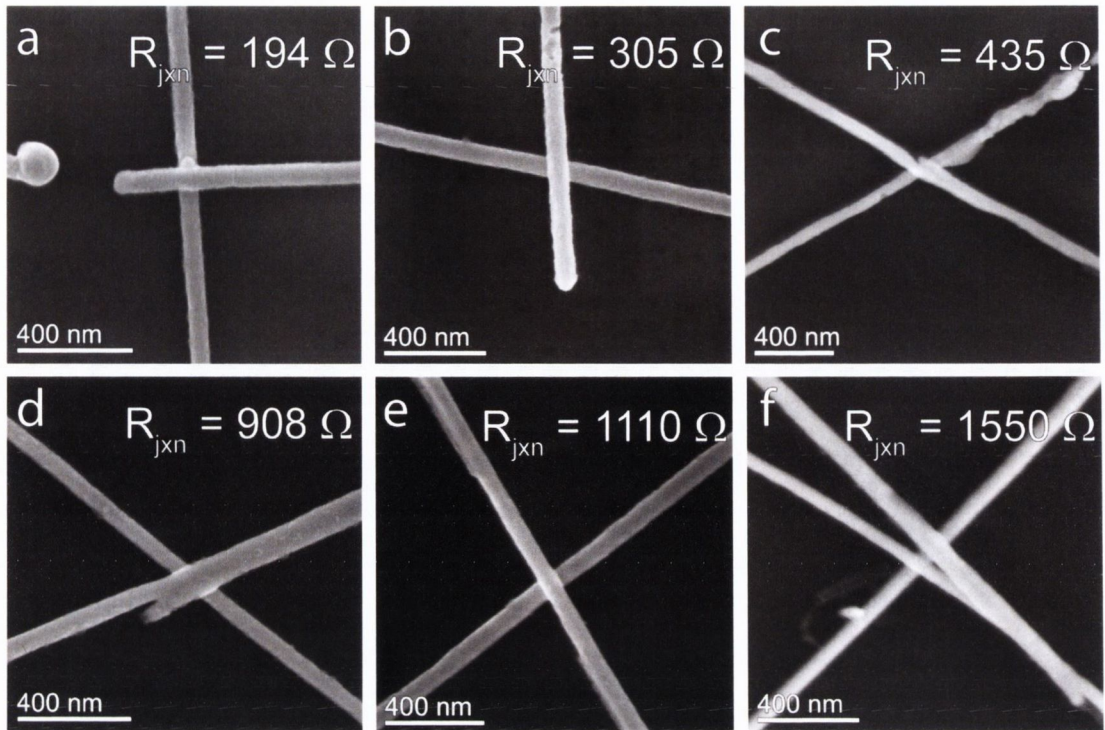
FIGURE 3.14. SEM analysis of measured Ni nanowire junctions. Junctions are arranged left-to-right in order of lowest R_{jxn} value obtained. An example of the kind of catastrophic failure commonly observed in these systems may be seen in panel (a), while partial failure is visible in (c).

how the value of R_{jxn} varies between cycles. In both cases it can be seen that there is significant variance in R_{jxn} from cycle to cycle, differing by as much as 100%. This is a particularly interesting result, as based on the work on quantized conductance atomic switches,[22] it may be assumed that the variation in R_{jxn} is a direct measure of the variation in the conductive filament, that is, the lower the resistance, the thicker/wider the filament. These nanostructures are extremely fragile, and are prone to failure when placed under electrical stress, such as the large current densities experienced during the reset step. As a result, very few junctions were found to be capable of multiple RS cycles, hence only two are shown here.

The Ni nanowire junctions for which R_{jxn} was measured were characterised with SEM – see Figure 3.14. From these images, there appears to be no morphological reason for the distribution of R_{jxn} values observed. Each junction was formed to the same current level, and should therefore have experienced similar current densities and associated Joule heating effects. It is well known that resistive switching materials display significant distributions in switching parameters, including resistance of the LRS. These systems are therefore extremely complex, and much more in depth analysis is required to determine the true origin of the variation in values obtained.

3.3.3 Outlook

The measurements of the resistance of single nanowire junctions presented in this chapter have improved our understanding of these nanoscale interfacial systems. The R_{jxn} for Ag nanowires was found to be considerably lower than reported elsewhere for similar measurements. By performing measurements on a range of junctions, which were "activated" through both thermal and electrical means, a distribution of R_{jxn} values was determined, with a median value of only 23 Ω. This has important implications for those working in the field of nanowire networks, particularly for transparent conductor applications. Simulations that have been performed thus far on these systems have overestimated the contribution of the junction to the total resistance of the network. Therefore, using these results it should be possible to adjust the current simulation models to reflect the new findings, and thereby establish a universal model for the simulation and analysis of networks of nanowires. Furthermore, using such a universal model it will be possible to simulate accurately the properties of a nanowire network of any material, as long as critical parameters such as R_{jxn} are known. To this end, measurements on Ni nanowire junctions have been presented in this chapter. Ni nanowires are an intriguing material from the point of network fabrication as they possess a native passivating oxide which may be penetrated with the action of an electric field, thereby creating an ohmic connection between nanowires which is naturally resistant to atmospheric degradation.

3.4 Impedance Spectroscopy of Single Nanowire Junctions

The final section in this chapter focuses on utilising impedance spectroscopy to study the properties of nanowire junctions. Impedance spectroscopy is a challenging technique requiring precision measurements coupled with a finely calibrated measurement system and informed analysis in order to extract the most important, and relevant physical parameters. This is particularly so for measurements on the nanoscale. The details of the measurement set-up and calibration, as well as the challenges and limitations associated with such precision measurements are described, and some initial results presented.

Motivation

The Ag/PVP/Ag nanowire junction as well as the Ni/NiO/Ni junction may be described, in their most basic form, as simple capacitors that undergo electrical breakdown at a voltage, v_B. A nanowire network may then be described as a network of capacitors, with a distribution of breakdown voltages, $\rho(v_B)$, and application of a voltage across such a network will cause breakdown of the weakest junctions, similar to the breakdown of a dielectric along the grain boundaries, i.e. the lowest energy path. Chapters 4 and 5 will delve into these concepts in detail, probing the DC electrical properties of these networks. For now however, it suffices to say that DC measurements may only probe the properties of a junction, or a network, once an ohmic connection has been formed between the interrogating electrodes. No

information is gained about the physical and chemical processes that are occurring during the activation process.

Impedance spectroscopy however may provide a window to these complex events. In the context of single junctions, a greater understanding of the breakdown processes may be gained, and in the context of networks of nanowires, insight may be gained into the activation of junctions prior to formation of a conductive pathway spanning the network. By mapping the change in network capacitance with applied voltage, unseen internal changes within the network may be probed. This will improve our understanding of the behaviour of networks, and thus will lead to further developments in networks as a materials technology.

Before measurements of complex networks may be performed, initial measurements of single junctions must first be made, both to understand the limitations of the technique on a much simpler system, but also to gain insight into the junction properties in both ON and OFF states and extract an equivalent circuit. This section begins by focusing on the measurement details, and will conclude with initial results.

3.4.1 MEASUREMENT SET-UP & COMPENSATION

Electrical system II, described in chapter 2, was used to perform the impedance measurements presented here. A capacitance-voltage unit (CVU), with four unknown terminals (HI Cur, HI Pot, LO Cur, and LO Pot), connects to the sample by means of coax SMA cables, triax cables, and finally by contacting the sample with tungsten probe needles. This is schematically illustrated in Figure 3.15. The CVU is calibrated in the factory up to the unknown terminals, however beyond this the user must perform their own calibration prior to each measurement. Each cable has associated with it a lead inductance, similarly cable pairs have an associated capacitance. These are collectively known as residual impedance, and if not accounted for can result in distorted measurements by effectively adding a parasitic component to the device under test (DUT). By carefully designing the connections however, some residuals may be eliminated. For example, the capacitance between SMA or triax cables may be eliminated by connecting the grounded shields close to the DUT, as shown in Figure 3.15. The residual capacitance of the cables is then reduced to only the remaining length of exposed cable – in this case the tungsten probes. This distance is made as short as possible to improve measurement accuracy.

While measurement set-up may remove some residual impedance from the measurements, some will always remain. To account for this, compensation techniques are used to remove the effect of known residuals from the measured data. This is done in four different ways: open, short, cable, and load compensation. Open compensation measures the stray admittance, Y_O, where $Y_O = G_O + j\omega C_O$, when the circuit is open. Short compensation measures the residual impedance, Z_S, where $Z_S = R_S + j\omega L_S$, when the circuit is shorted. By accounting for these residuals, the measurement system may calculate the DUT impedance,
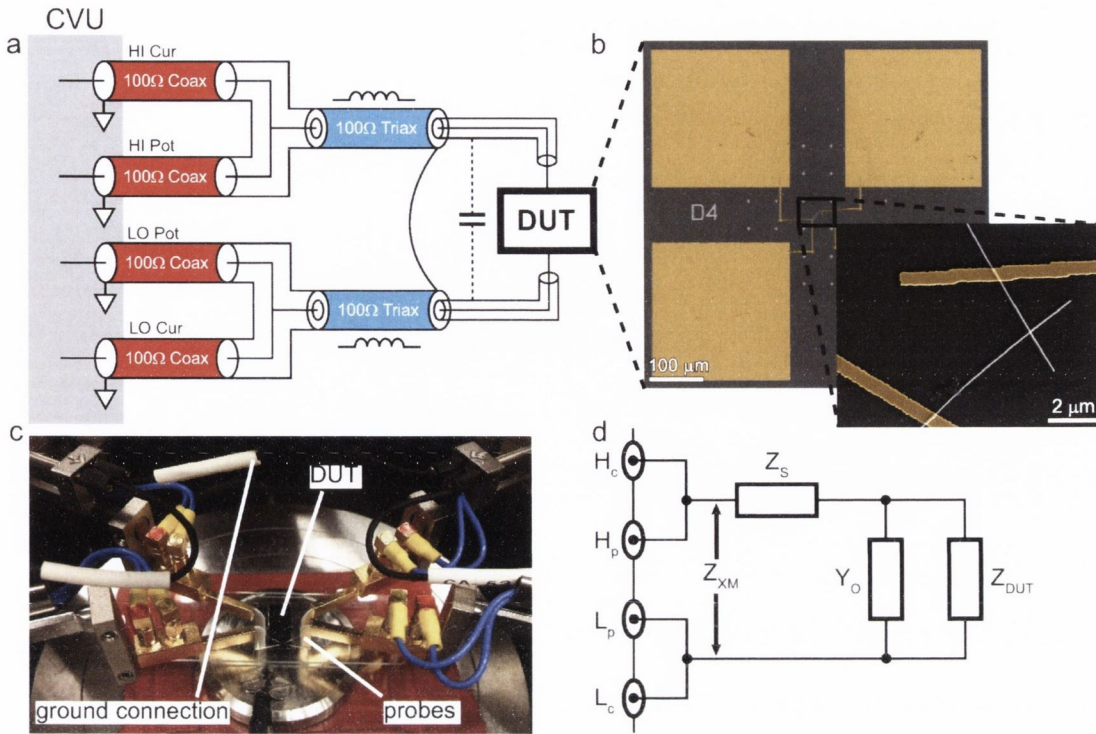
FIGURE 3.15. Set-up of impedance measurements on a single nanowire junction. (a) Schematic of connections between CVU module and the device-under-test (DUT), illustrating sources of residual impedance. (b) SEM images of the DUT (nanowire junction). Electrodes are false coloured for clarity. (c) Photograph showing the contact to the DUT via W probes. A cable connects the shields of the HI and LO terminals, as depicted in (a). (d) Simplified equivalent circuit of the measurement showing the residual impedance, Z_S, stray admittance, Y_O, measured impedance, Z_{XM}, and the desired impedance, Z_{DUT}.

Z_{DUT} according to the equation:

$$Z_{DUT} = \frac{Z_{XM} - Z_S}{1 - (Z_{XM} - Z_S)Y_O} \tag{3.1}$$

where Z_{XM} is the measured impedance.[23] Z_{XM}, Y_O, Z_S, and Z_{DUT} are schematically shown in Figure 3.15(d).

The instrumentation must also take into account the impedance of the cables being used to make the measurement. This is done by specifying the cable length for standardised cables (for example, SMA coax cables have a characteristic impedance of 50 Ω), however additional cables and connections will increase the cable length, and therefore a cable length compensation measurement is required. This is performed by sending a signal down an open cable and measuring the time required for the reflected signal to return. Finally load compensation is used where more complex parasitic circuits are affecting the measurement, and open/short compensation methods are not sufficient. Load compensation adds a load of known magnitude, which should be close to that of the DUT, into the circuit in place of the DUT in order to measure more accurately the residuals and account for them in the final

FIGURE 3.16. Bode plot of $|Z|$ and θ for a Ni nanowire junction in (a) the pristine state, and (b) the LRS for the frequency range 1 kHz – 1 MHz. Both data sets display an RC series circuit behaviour, however the capacitance behaviour in (a) has been almost completely bypassed in (b), showing purely resistive behaviour, indicated by the phase angle of 0°.
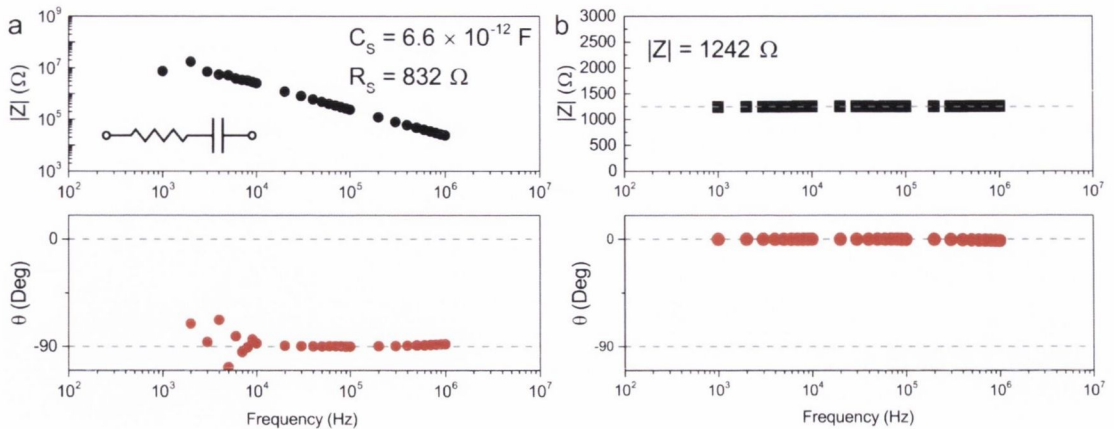
measurement.

3.4.2 NI NANOWIRE JUNCTION

Impedance measurements were performed on the same Ni nanowire junctions described in section 3.3.2, in parallel with the DC measurements. A Bode plot showing the impedance modulus, $|Z|$, and phase angle, θ, as a function of frequency is shown in Figure 3.16 for a Ni nanowire junction in both the pristine state and the LRS, in the frequency range 1 kHz – 1 MHz. For this measurement only open and cable compensation are applied, where the open compensation measurement was performed by lifting the probes from the sample. The plot shape in Figure 3.16(a) indicates an RC series circuit, and the capacitance may be extracted from the slope according to equation (2.11). A series capacitance of 6.6 pF, and a series resistance of 832 Ω were determined from this plot. Figure 3.16(b), showing the LRS data, also displays RC series circuit behaviour, however the phase angle of 0° is characteristic of purely resistive behaviour, indicating that the capacitive impedance has been removed. The 2-probe DC resistance measured for this state was 1389 Ω, very similar to the total impedance ($|Z|$) measured of 1242 Ω. It thus seems reasonable to conclude that in the LRS, the circuit can be approximated as a single resistor.

An additional measurement was performed once the nanowire had been switched into the HRS, shown in Figure 3.17, for the frequency range 1 kHz – 1 MHz. The data is displayed as both a Bode plot, as well as a Nyquist plot where the imaginary component of the impedance is plotted as a function of the real component. The shape of both plots indicates an RC parallel circuit behaviour – the characteristic semicircular Nyquist plot is indicative of an RC parallel circuit. For a simple parallel circuit such as that illustrated inset in Figure 3.17(a), the values of R1 and R2 may be found from the x-axis intercepts as shown in (b). R1 was found to be 2.2 kΩ, while R2 was found to be 342 kΩ – a 2-probe DC
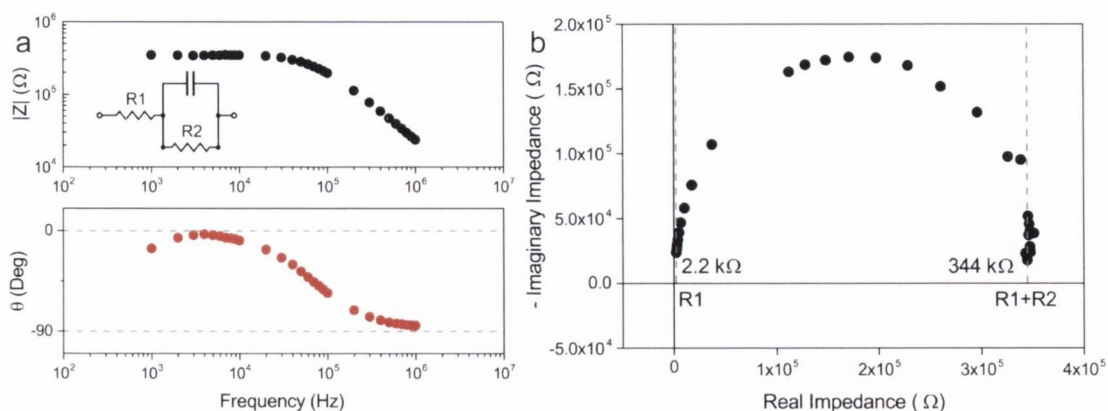
FIGURE 3.17. Bode (a) and Nyquist (b) plots of a Ni nanowire junction in the HRS. Both plots indicate an RC parallel circuit, such as that inset in (a). A semi-circular shape in the Nyquist plot is characteristic of RC parallel behaviour. The values R1 and R2 may be extracted from the x-axis intercepts, as shown.

measurement determined the resistance to be 348 kΩ. The capacitance was determined by fitting the data using the LEVM program described in chapter 2,[24] and was found to be 6.6 pF – equal to that measured for the pristine state.

Section 3.4.1 described the potential parasitic contributions to the measured impedance in terms of the cables alone, however the sample itself may introduce significant parasitic pathways that can drastically alter the measurement result. Figure 3.18 illustrates the parasitic capacitance resulting from the sample substrate used in this work. 300 nm of thermally grown SiO_2 lies on a heavily doped n-type Si substrate, adding a capacitance in parallel with the sample. For an electrode area of 250×250 μm^2, a simple calculation of the capacitance of two series capacitors, such as that shown in Figure 3.18, gives a value of 3.5 pF. For comparison, the capacitance of a single junction was estimated. For simplicity, the overlap area of two crossed nanowires, each 80 nm in diameter, was assumed to be between 5×5 nm^2 and 80×80 nm^2. By estimating the thickness of the NiO layer to be 12 nm, and using the relative permittivity for NiO of 11.9,[25] the capacitance is calculated to fall in the range 2×10^{-19} F to 6×10^{-17} F. Capacitances on this order are extremely challenging with even the most sophisticated systems. It is clear then that the series capacitance measured for the pristine state nanowire, and that measured in parallel
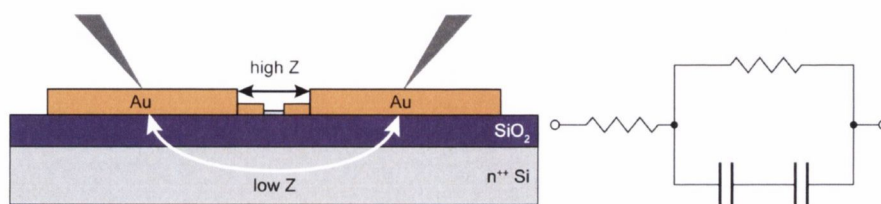
FIGURE 3.18. Illustration of parasitic capacitance introduced by sample substrate, and the equivalent circuit this approximates to.
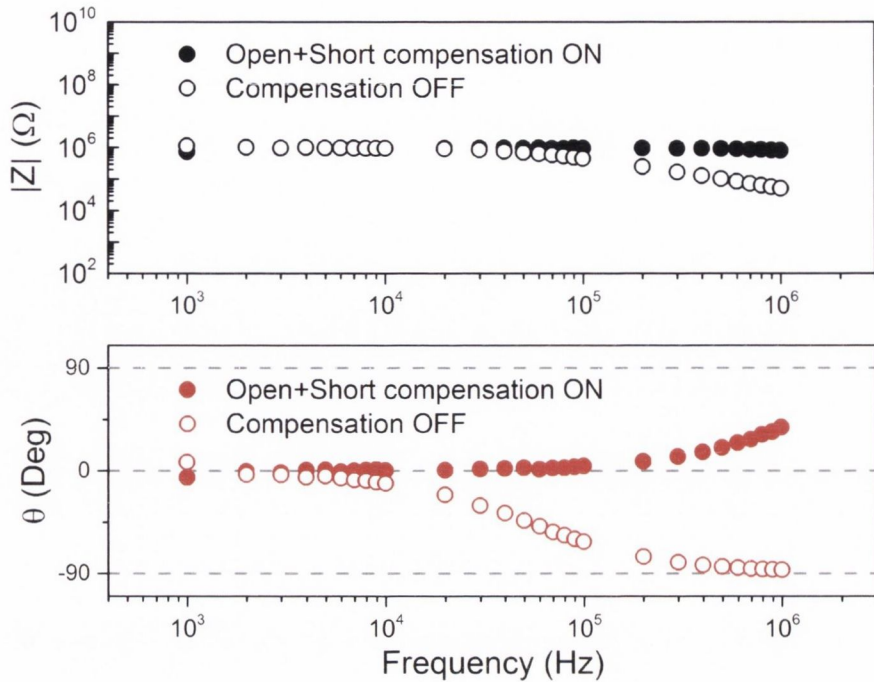
FIGURE 3.19. Fully calibrated impedance measurement of Ni nanowire junction in HRS.

for the LRS were the contributions of the substrate. As stated above, the compensation methods implemented prior to acquisition of the above data were quite basic, and thus more specific compensation methods are required to remove the effects of the substrate.

To account for the parasitics associated with the substrate, a dedicated calibration sample was fabricated by creating EBL defined Au electrodes on a standard substrate to emulate a contacted nanowire sample. This sample contained both open and short compensation structures. For the open compensation structure, the electrodes were defined approximately $2 \mu m$ apart in an open configuration, while they were connected for the short compensation structure. Using this calibration sample, open, short, and cable compensation were all implemented. The HRS of a Ni nanowire junction was then measured both with these compensation methods and without, for comparison. Figure 3.19 shows the results of this measurement.

By analysing the phase plot in the Figure 3.19, it can be seen that upon implementation of the open and short compensation methods, the capacitive behaviour – indicated by a phase angle of -90° – has been removed. The phase rises into positive values at higher frequencies, which may be an effect of overcompensation, perhaps as the measured sample and calibration sample were fabricated separately and thus there were some small differences that are amplified at the higher frequencies.

From these initial measurements, a number of conclusions may be drawn. Firstly, it is clear that in order to extract valuable information from impedance measurements appropriate calibration and compensation methods must be employed. Furthermore, it is necessary to fabricate dedicated calibration samples for each nanowire junction device to be measured,

and that they should mirror the sample as closely as possible to obtain the most accurate calibration. With regard to the measurements performed on a Ni nanowire junction, no information was obtained for the pristine state as the parasitic capacitance of the sample dominated the measurement. In the case of the LRS, the nanowire junction dominated the results, showing purely resistive behaviour in the chosen frequency range. Prior to implementing sample-specific compensation, the HRS of the junction initially displayed RC parallel circuit behaviour, however once the compensation was applied the measurement displayed largely resistive behaviour, the magnitude of which was approximately equal to the 2-probe measured resistance. These results indicate that the impedance analysis of nanowire networks may be a viable technique for the analysis of large networks when appropriate measurement compensation is applied, however the capacitance of a single junction is simply too small to be measured using the current characterisation system.

3.5 Conclusions

This chapter has presented results of the electrical measurements on single junctions between pairs of Ag and Ni nanowires. The most comprehensive study of single Ag nanowire junctions to date was performed, and it was found that a wide distribution of resistance values exist, having an average of 58 Ω and a median value of 23 Ω. Both annealed and electrically activated junctions were measured, and it was found that electrical activation is capable of generating very low junction resistances without inducing morphological changes. These results have significant implications for the future study of Ag nanowire networks, in particular the simulation of these networks. The junction resistance of Ni nanowire junctions was also measured, and it was found that these junctions are significantly more resistive that those of Ag, having a average resistance of 718 Ω. This was attributed to the nanoscale conductive filament that must be formed through the native NiO layer coating each nanowire. Additionally, the variation in the junction resistance was measured for multiple resistive switching cycles, giving insight into the variation in the width of the conductive filament. Finally, impedance measurements of single Ni nanowires were performed. It was found that, with appropriate compensation for parasitic impedance, impedance spectroscopy may be a viable technique to analyse large networks of capacitive junctions, but that single junctions are immeasurable with current technology.

REFERENCES

[1] DE, S., HIGGINS, T. M., LYONS, P. E. ET AL., *ACS Nano* **2009**, *3*, 1767–1774.

[2] SOREL, S., LYONS, P. E., DE, S. ET AL., *Nanotechnology* **2012**, *23*, 185201.

[3] PRESTON, C., XU, Y., HAN, X. ET AL., *Nano Research* **2013**, *6*, 461–468.

[4] LANGLEY, D., GIUSTI, G., MAYOUSSE, C. ET AL., *Nanotechnology* **2013**, *24*, 452001.

[5] LEE, J.-Y., CONNOR, S. T., CUI, Y. ET AL., *Nano Letters* **2008**, *8*, 689–692.

[6] MUTISO, R. M., SHERROTT, M. C., RATHMELL, A. R. ET AL., *ACS nano* **2013**, *7*, 7654–7663.

[7] HU, L. B., KIM, H. S., LEE, J. Y. ET AL., *ACS Nano* **2010**, *4*, 2955–2963.

[8] GARNETT, E. C., CAI, W., CHA, J. J. ET AL., *Nature Materials* **2012**, *11*, 241–249.

[9] SONG, T.-B., CHEN, Y., CHUNG, C.-H. ET AL., *ACS Nano* **2014**, *8*, 2804–2811.

[10] RATHMELL, A. R., NGUYEN, M., CHI, M. F. ET AL., *Nano Letters* **2012**, *12*, 3193–3199.

[11] CHEN, Z., YE, S., STEWART, I. E. ET AL., *ACS nano* **2014**.

[12] CAGLI, C., NARDI, F., HARTENECK, B. ET AL., *Small* **2011**, *7*, 2899–2905.

[13] *Seashell Technology, LLC*, http://www.seashelltech.com/.

[14] WILEY, B., SUN, Y., MAYERS, B. ET AL., *Chemistry-A European Journal* **2005**, *11*, 454–463.

[15] GAO, Y., JIANG, P., SONG, L. ET AL., *Journal of Physics D: Applied Physics* **2005**, *38*, 1061.

[16] *Nanomaterials.it*, http://www.nanomaterials.it/.

[17] KOLEŚNIK, M. M., HANSEL, S., LUTZ, T. ET AL., *Small* **2011**, *7*, 2873–2877.

[18] JEONG, D. S., SCHROEDER, H., and WASER, R., *Electrochemical and solid-state letters* **2007**, *10*, G51–G53.

[19] KIM, K. M., JEONG, D. S., and HWANG, C. S., *Nanotechnology* **2011**, *22*, 254002.

[20] HE, L., LIAO, Z.-M., WU, H.-C. ET AL., *Nano Letters* **2011**, *11*, 4601–4606.

[21] KWON, D.-H., KIM, K. M., JANG, J. H. ET AL., *Nature nanotechnology* **2010**, *5*, 148–153.

[22] TERABE, K., HASEGAWA, T., NAKAYAMA, T. ET AL., *Nature* **2005**, *433*, 47–50.

[23] *Agilent Impedance Handbook: A guide to measurement technology and techniques*, Agilent Technologies, 4th edition, **2013**.

[24] MACDONALD, J. R., *LEVM Complex Nonlinear Least Squares Fitting Program*,

http://www.jrossmacdonald.com/levminfo.html, **2012**.

[25] RAO, K. and SMAKULA, A., *Journal of Applied Physics* **1965**, *36*, 2031–2038.

MANIPULATING CONNECTIVITY & CONDUCTIVITY IN Ag NANOWIRE NETWORKS

In chapter 3, it was established that PVP-coated Ag nanowires are non-conducting in the pristine, as-synthesized state, and that this state may be switched by both thermal and electrical means to create junctions with extremely low resistances. Thermal annealing is a common step performed on networks of nanowires to reduce the junction resistance and obtain fully connected, high conductivity networks. The electrical activation of networks however, has not been studied to date, and it is thus not understood how a network of coated nanowires behaves under electrical stress. The results of this chapter show that the study of the behaviour of such materials can provide insight into the mechanisms controlling the properties of random networks, as well as uncovering previously undiscovered phenomena. Specifically, it is shown that a network of PVP-coated Ag nanowires placed under electrical stress distributes this stress through the evolution of connectivity, giving rise to a material whose resistance may be arbitrarily tuned. Part of the work presented in this chapter has been published in the journal *Nano Letters*.[1]

4.1 PREFACE: NETWORK ACTIVATION

4.1.1 CONDUCTIVITY MAPPING IN Ag NANOWIRE NETWORKS

In order to investigate the electrical activation of Ag nanowire networks, a conductive atomic force microscopy (CAFM) study was performed by Dr Peter Nirmalraj to investigate the connectivity between a nanoscale point in the network and a much larger planar electrode. As described in chapter 2, CAFM simultaneously maps the topography and electrical conductivity of a sample by biasing a conductive AFM tip relative to the sample, and measuring the very small current response. An illustration of a CAFM experimental set-up is shown in
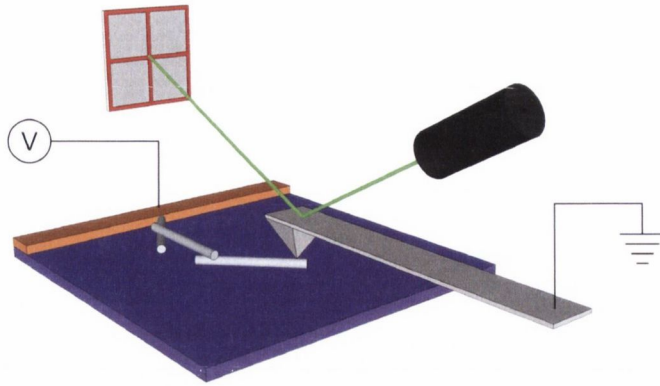
FIGURE 4.1. Schematic illustration of a CAFM experimental set-up. A conductive tip is biased relative to the substrate, allowing simultaneous mapping of both the topography and conductivity.

Figure 4.1.

Figure 4.2 shows the results of this CAFM study. A Ag nanowire network, contacted by a planar, Pt electrode via shadow masking (top of images, not shown), is biased relative to the Pt coated AFM tip placed in contact with the network. In agreement with the results of chapter 3, it was found that in the initial state, the network was non-conducting at a bias of 200 mV due to the presence of the insulating PVP coating at the nanowire junctions. Performing a linear voltage sweep across the network, a threshold voltage, V_T, was found beyond which current flowed through the network and into the tip, consistent with the results obtained for single junctions. The power of the CAFM technique is that conductivity maps may be generated and allow the electrical connectivity in complex materials such as a nanowire network to be visualised. To this end, a detailed topography scan was obtained of a 60×60 µm area, shown in Figure 4.2(a). Following this the AFM tip, acting as a mobile electrode, was placed at position 1 in Figure 4.2(a) and a 6 V, 2 second pulse was applied, after which the network was re-imaged in CAFM mode. This pulse scheme was chosen to be much greater than V_T, and therefore was likely to activate wires within the network. This process was repeated for positions 2 – 5 in Figure 4.2(a).

Figure 4.2(b – f) shows the conductivity maps that resulted after each successive pulse, imaged at a low bias of 200 mV. It is clear that following each pulse, more wires become activated and are visible in the conductivity maps, indicating that the PVP has been broken down and the nanowires are now electrically connected to each other and to the planar electrode. This implies the electrical stimulus is directly modifying the connectivity of the random nanowire network. It is also clear that nanowires surrounding the contact point are also activated, and not just simply those in a direct line to the electrode.

It is interesting to note that the PVP coating fully encapsulates the nanowires, and therefore should prevent electrical contact between the AFM tip and the Ag core of the nanowire. One would then expect the nanowires to still appear invisible in conductivity maps, even if the PVP at the junction has been broken down following a pulse. However,
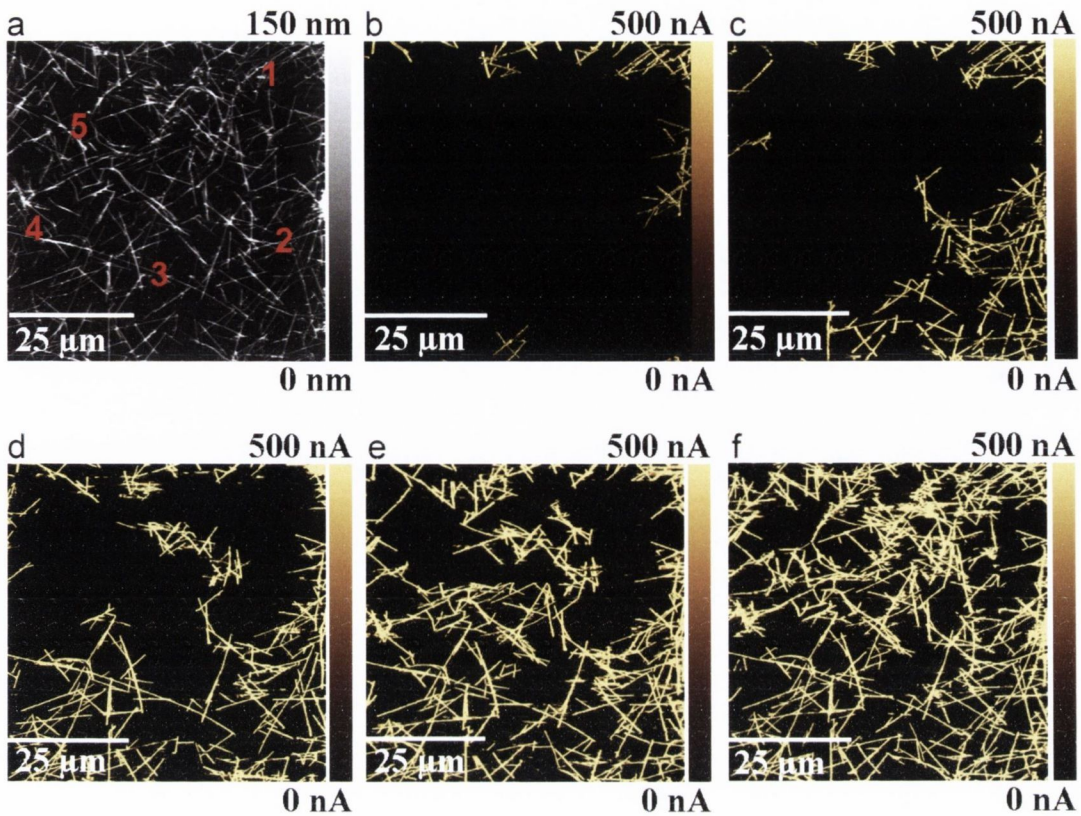
FIGURE 4.2. CAFM study of Ag nanowire networks. (a) Topographic image of a network. (b) Conductivity map of network shown in (a) after a 6 V, 2 s pulse at position 1. Planar electrode is at top of image, not shown. (c – f) Conductivity maps after pulses at positions 2 – 5. Successive pulsing creates conductive pathways between AFM tip and electrode, seen in the images as bright nanowires.

as CAFM is a contact-mode AFM technique, high forces (~ 50 nN) are applied between the tip and sample and it is therefore likely that the tip penetrates the thin PVP coating during imaging, enabling current to flow through the nanowire core. Another hypothesis for this result is that the sudden current flow through the nanowires causes the thermal breakdown of the PVP coating via Joule heating, thereby creating a clean Ag surface with which the AFM tip can make contact.

The voltage threshold for conduction, V_T, shows a strong dependency on the distance of the AFM tip to the electrode, demonstrated in Figure 4.3 (a) and (b). There is also a dependency of the voltage threshold on the nanowire density, N/A, as shown in Figure 4.3(b), which indicates that V_T is proportional to the number of junctions per nanowire. The data in (b) can be replotted to show V_T as a function of N/A. The result fits well to a power law with exponent, n. Figure 4.3(c) plots this exponent as a function of the interelectrode distance, D. At small D n is equal to -1 and quickly rises to a value of -0.5 at larger D values.

FIGURE 4.3. Scaling of V_T with electrode-tip distance, D. (a) I-V plot showing the activation of a Ag nanowire network at two inter-electrode distances: 100 μm and 700 μm. The activation voltage, V_T appears to scale with D. (b) V_T plotted as a function of D for networks of varying density, from $0.08 - 1.00$ NW/μm^2. (c) Data in (b) replotted to show the power law exponent, n, as a function of D. At small D, $n = -1$ but quickly rises to $n = -0.5$ with increasing D.
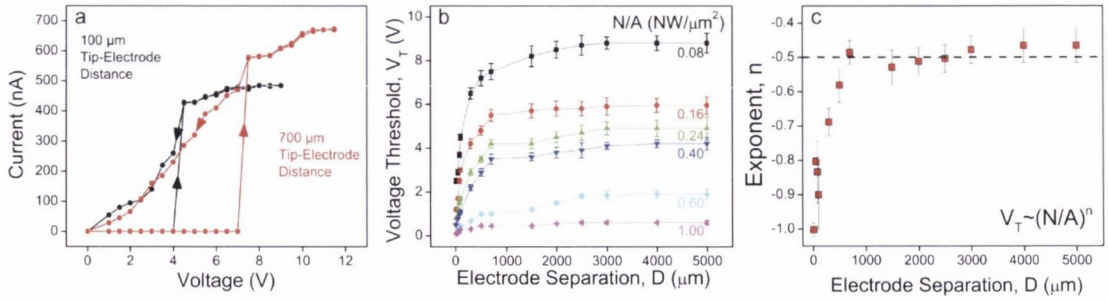
4.1.2 NETWORK ACTIVATION MODEL

To investigate how a random network such as the one described above will connect between the AFM tip and the planar electrode, a model was developed by the Ferreira and Coleman groups in the Physics department.

The network may be thought of as a leaky resistor-capacitor network with randomly positioned junctions, where $\rho(v_B)$ is the distribution of breakdown voltages, v_B. Upon application of a voltage, V, a number of weaker junctions will be broken down regardless of whether a conductive path is formed between electrodes. The number of broken junctions, $N_{J,B}$, per area is given by:

$$\frac{N_{J,B}}{A} = \frac{N_J}{A} \int_0^v dv_B \rho(v_B) \tag{4.1}$$

where N_J/A is the total junctions per area. The average distance between activated junctions, $\langle d_B \rangle$, is then

$$\langle d_B \rangle \approx \left(\frac{A}{N_{J,B}} \right)^{1/2} \tag{4.2}$$

A network with these properties is simulated by considering a random ensemble of nanowires within a two-dimensional box of arbitrary size. Charge will only flow across a junction (considered as a capacitor) if the voltage across it exceeds v_B for that junction. Once this occurs, neighbouring nanowires experience a redistribution of voltages. Simulations reveal that this redistribution results in a cascade effect creating a localised activation cell, of radius R_C, that is bordered by junctions with higher values of v_B, as defined by $\rho(v_B)$. The radius of the cell will depend on the applied voltage, V, according to

$$R_C = aV^\alpha \tag{4.3}$$

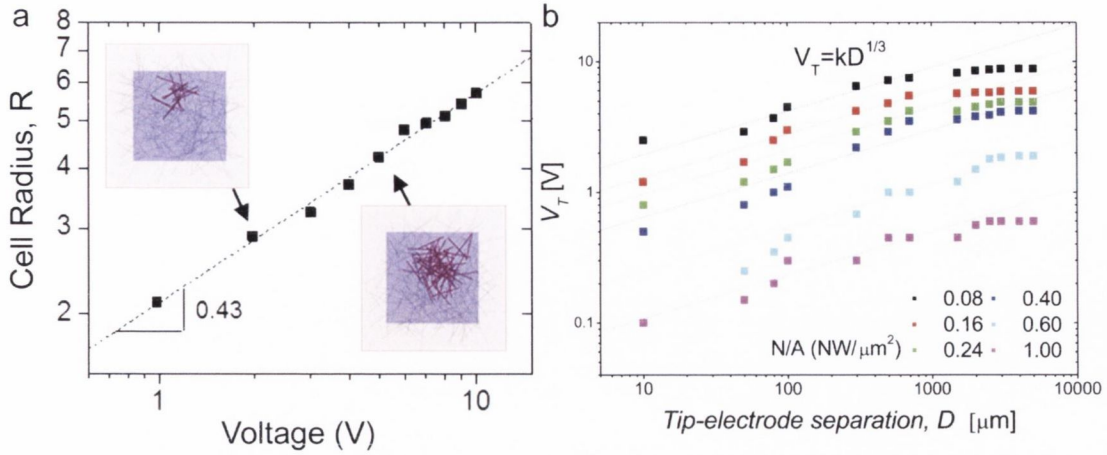where α and a are constants.

FIGURE 4.4. (a) Simulation of connectivity cell scaling, and (b) V_T replotted as a function of D to show the $V_T \propto D^{1/3}$ relationship.

The global threshold voltage, V_T, is reached when activation cells grow such that they overlap adjacent cells, that is when $\langle d_B \rangle \approx R_C$. Following from this, and combining equations (4.1) to (4.3), we get:

$$ a V_T^\alpha = \left[\eta \frac{N}{A} \int_0^v d v_B \rho(v_B) \right]^{-1/2} \tag{4.4} $$

where η is the number of junctions per wire.

For the case that the interelectrode distance, D, is very small, it is possible to obtain a relationship between V_T and N/A. For very small D, such that a single activation cell spans the width of the electrodes, or $R_C \geq D$, it is assumed that the bounding values of v are quite large, thus allowing the cell to be big, which allows us to approximate $\int_0^v d v_B \rho(v_B)$ as being independent of v. Additionally, the experiment shows that at small D, $V_T \propto (N/A)^{-1}$; which means that the value of α must be 0.5. Simulations reveal that R_C does in fact scale with V to a power law (see Figure 4.4(a)), and show an exponent $\alpha = 0.43$, in very close agreement to that predicted by the theory.

A similar analysis to that above shows that at large D, $V_T \approx D^{1/3}$ – see appendix A for full proof. This is confirmed by re-plotting the data in Figure 4.3(b) in log-log form (see Figure 4.4(b)). The data scales as $V_T = kD^{1/3}$ for medium values of D, confirming the theory. At very large D, this relationship is expected to break down as the distribution $\rho(v_B)$ begins to deviate from a simple power law expression.

The results of the CAFM study and the model developed subsequently provide critical insight into the connectivity behaviour of a random network. The "activation cell" based model predicts experimental results remarkably well, and has some interesting implications for such systems, such as the existence of clusters of activated nanowires which do not contribute to the initial conducting pathway, but are created simply as a result of a sufficient voltage drop across the junction. This is shown in the following sections to play an important
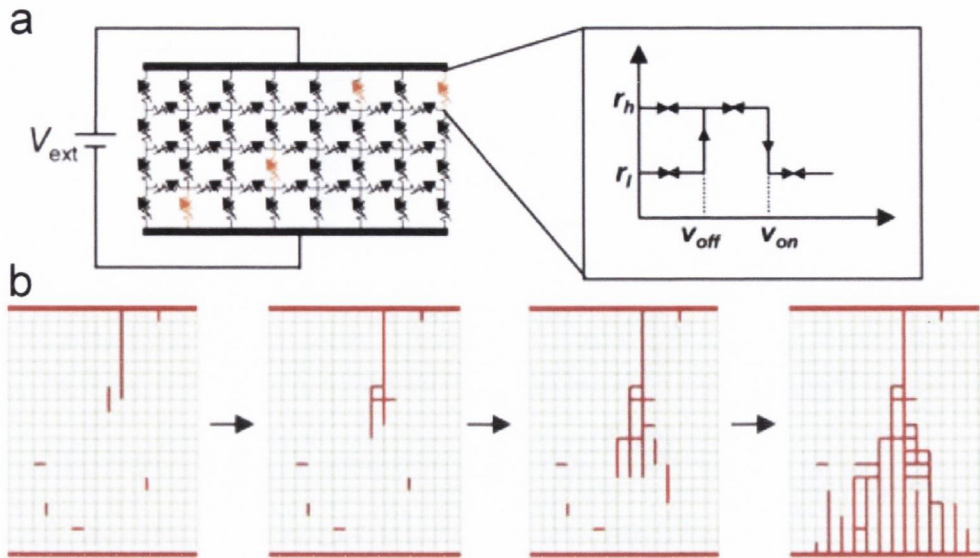
FIGURE 4.5. Random circuit breaker model developed by Chae et al. describing the electroforming in a TiO$_2$ resistive switch.[2] (a) Schematic of circuit breaker arrays (b) Progression of conductive pathways connected by on-state circuit breakers may be described by an avalanche breakdown mechanism.

role in the behaviour of the network post-activation.

In the context of this result, it would be remiss not to include a discussion of other models developed to describe the formation of conductive pathways in other network systems. One space where this is of particular relevance is the field of resistive switching, and in particular the modelling of the electroforming step. In 2008, Chae et al. developed a random circuit breaker (RCB) model to describe the electroforming in a Pt/TiO$_2$/Pt system.[2] In this model they describe the system as a 2-D array of circuit breakers, each having one of two resistances – R_h and R_l, where $R_h \gg R_l$. The state of each circuit breaker may change if the voltage, Δv, across it is of a sufficient magnitude, such that:

$$\text{off-state} \rightarrow \text{on-state when } \Delta v > v_{on}$$

and

$$\text{on-state} \rightarrow \text{off-state when } \Delta v > v_{off}$$

where $v_{on} \gg v_{off}$. In the case of the model developed in this work, no transition to an off-state is considered, as the electrical breakdown of PVP is assumed to be irreversible. The RCB model was shown to be capable of accurately describing the formation of the conductive filament in a resistive switch as the voltage across the network was swept, and was also capable of demonstrating the variation in V_{SET}, V_{RESET}, and V_{FORM} commonly associated with unipolar resistive switches. Figure 4.5 shows an example of this RCB model.

One crucial difference between the model described in this work and that developed by Chae et al. is the inclusion of a breakdown voltage distribution, $\rho(v_B)$. This critical

parameter allows for the formation of self-limiting cells bounded by junctions with v_B values at the higher end of the distribution, and its inclusion also appears to be a more accurate physical description of a random nanoscale system. The reset, or switching behaviour of metal oxide materials under electrical stress is well documented, and accounted for in the RCB model by the inclusion of a reset mechanism, where $v_{off} \ll v_{on}$. As Ag/PVP is not known to display such behaviour, no such reset mechanism is included in the developed model. However, the question then arises as to how a random nanowire network will behave when electrically stressed post-activation. The remainder of this chapter focuses on this question.

4.2 POST-ACTIVATION ELECTRICAL BEHAVIOUR

As highlighted above for the model developed by Chae et al., a nanowire network, modelled as a random arrangement of capacitors, has other nanoscale analogues such as insulating oxides used in the field of resistive switching. This implies that the electrical properties observed for nanowire network systems may be transferable to other nanoscale systems. To study the behaviour of these networks, the post-activation current-voltage behaviour is examined. As is shown in this section, the connectivity within an electrically formed random network is not a fixed quantity, but may be manipulated to give precise control of the network conductivity.

In order to investigate the post-activation electrical behaviour of Ag nanowire networks, a planar electrode geometry with two lateral contacts was employed, shown in Figure 4.6, rather than the CAFM technique described in the last section. Prior to the acquisition of a shadow mask with fine (sub 100 μm) features, two separate methodologies were adopted in order to fabricate these samples. For small networks (D < 100 μm), a bottom contacting approach was taken. Ti/Au (5/35 nm) electrodes were fabricated onto clean 300 nm SiO_2/Si substrates using EBL, such that the interelectrode distances were $D = 20$ μm and $D = 40$ μm respectively. Onto these a dilute solution of Ag nanowires (nominally 0.1 mg/ml) was sprayed by hand, such that the electrical contact was formed on the underside of the nanowires.

For large (D > 100 μm) networks, a nanowire dispersion was sprayed onto both 300 nm SiO_2/Si and glass substrates via the robotic spraying system described in chapter 2. UV-vis spectroscopy of the networks on glass substrates was used to determine the transmittance, T, at 550 nm and calibrate the nanowire dispersion (see Figure 4.7) for subsequent samples. Following network deposition, Ti/Au (5/35 nm) metal contact electrodes were deposited via the shadow masking technique. SEM and AFM images of these networks are shown in Figure 4.6. The networks were characterised according to the network size, D/L_{NW}, where L was taken to be the average nanowire length, measured in chapter 3. System-I was used for all electrical characterisation in this chapter (see section 2.4).
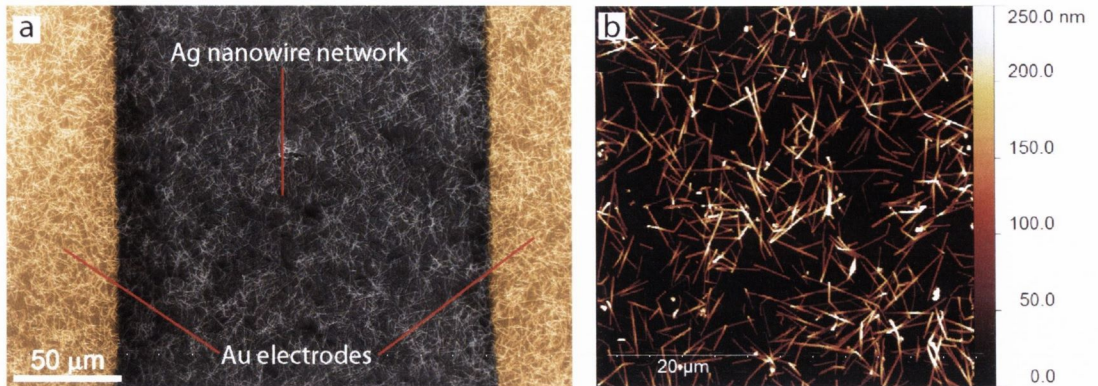
FIGURE 4.6. SEM and AFM images of Ag nanowire networks. (a) False coloured SEM image of a Ag nanowire network contacted with Ti/Au electrodes deposited via a shadow mask technique. Network shown has an approximate size of $D/L_{NW} = 24$ (a) AFM height image of a $T = 87\%$ network of Ag nanowires.
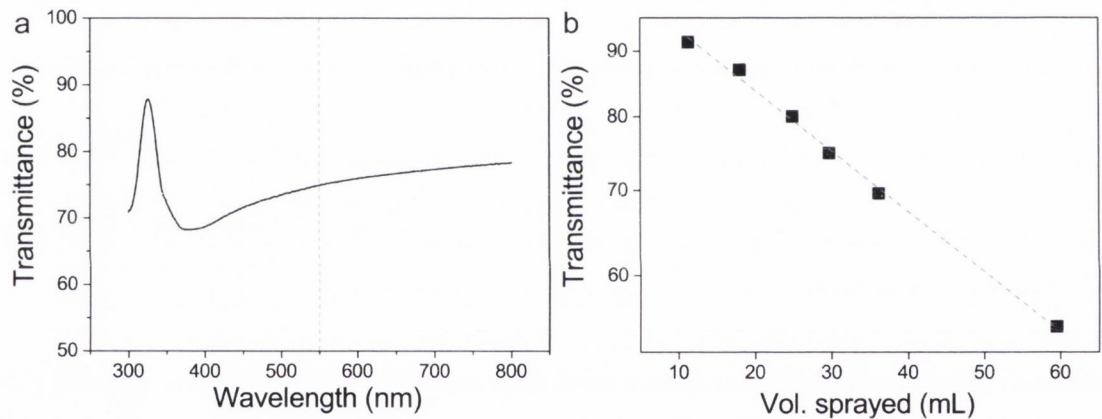
FIGURE 4.7. Calibration of Ag nanowire dispersion. (a) UV-vis spectrum of Ag nanowire network showing a transmittance of 75% at 550 nm. (b) Calibration curve. Transmittance at 550 nm plotted as a function of spray volume displaying a linear relationship.

4.2.1 SMALL NETWORKS: $D/L_{NW} = 2.74$

To begin, the electrical behaviour of a sparse network, where $D/L_{NW} = 2.74$, was investigated. Figure 4.8(a) shows the I-V curve for a 1.5 V linear sweep applied across the network shown in Figure 4.8(b). At low bias, no current is detected as the PVP coating impedes current flow through the junctions, consistent with results of single junctions in chapter 3 and the CAFM measurements presented in this chapter. At approximately 600 mV the current begins to rise steeply as the resistance of the network decreases, hitting the set compliance of 10 µA at 840 mV. The resistance was subsequently measured to be 16 kΩ, demonstrating that the network had formed a conductive pathway between the electrodes. Post-activation, the compliance current was removed and a bipolar voltage sweep to 600 mV was applied across the network. The resulting I-V curve is shown in Figure 4.9, black trace, plotted as
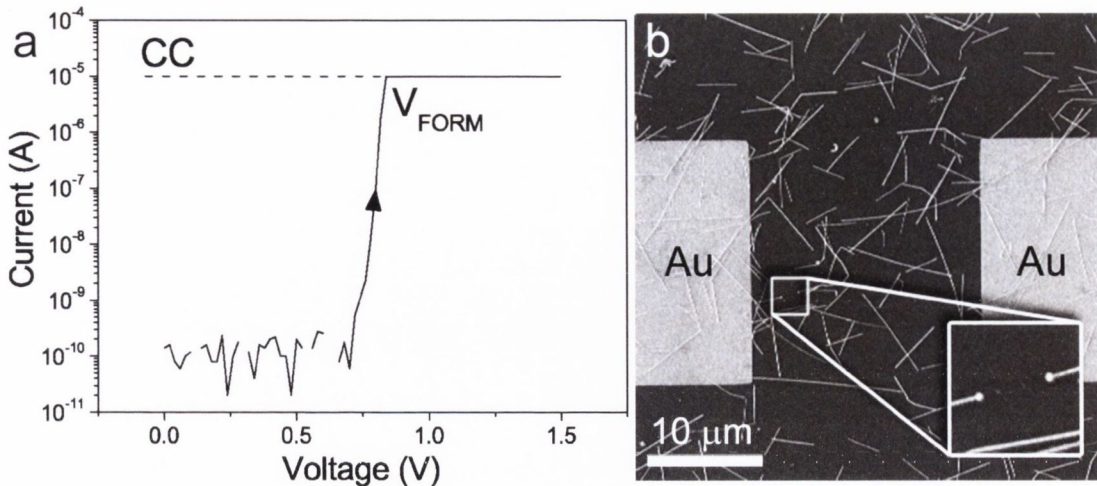
FIGURE 4.8. Electrical activation in a $D/L_{NW} = 2.74$ Ag nanowire network. (a) I-V curve showing the formation of a conductive pathway across the network. The detected current rises steeply at 600 mV hitting a compliance current of 10 µA at 840 mV. Sweep rate is $\sim$ 100 mV/s. (b) SEM of network activated in (a). Network is very sparse (T > 90%), bottom-contacted by Au electrodes shown. Inset shows magnified image of a failed nanowire, as explained in the text.

absolute current, where the inset illustrates the sawtooth nature of the voltage sweep. Large hysteretic current loops are visible at both positive and negative bias. The shape is not that of the "pinched hysteresis loop", which would be indicative of memristive behaviour,[3,4] but rather the current increases at both positive and negative bias as the resistance of the network reduces continually under the applied voltage.

The network was stressed further by performing subsequent sweeps, increasing the value of V_{max} in each case. The I-V curves show the hysteretic behaviour continues as V_{max} is increased, though the degree of hysteresis lessens with each subsequent sweep. It is also evident that there is a greater level of resistance change at positive voltage, though the behaviour is present for both positive and negative bias. It is also important to note that the resistance state of the network does not change when the bias is removed, indicating a permanent change in the network, and a demonstration of memory. The final sweep performed on this network is shown by the dark green trace in Figure 4.9, where the current can be seen to drop suddenly at 925 mV.

To explain this behaviour, it is helpful to revisit the activation theory developed in section 4.1. It was established that a random network becomes activated due to the formation of activation cells, and a conductive pathway through the network is formed when adjacent cells grow to the point that they overlap, that is, when $\langle d_B \rangle \approx R_C$. Thus outside of the initial percolating path, activation cells may exist that have not yet become connected to this path, and there will be a voltage, $v_{B,e}$, required to complete the connection. Associated with these cells then will be a distribution of voltages, $\rho(v_{B,e})$, a subset of $\rho(v_B)$, required to connect these activation cells to the main conducting path. It is also likely that $\rho(v_{B,e})$ exists in the
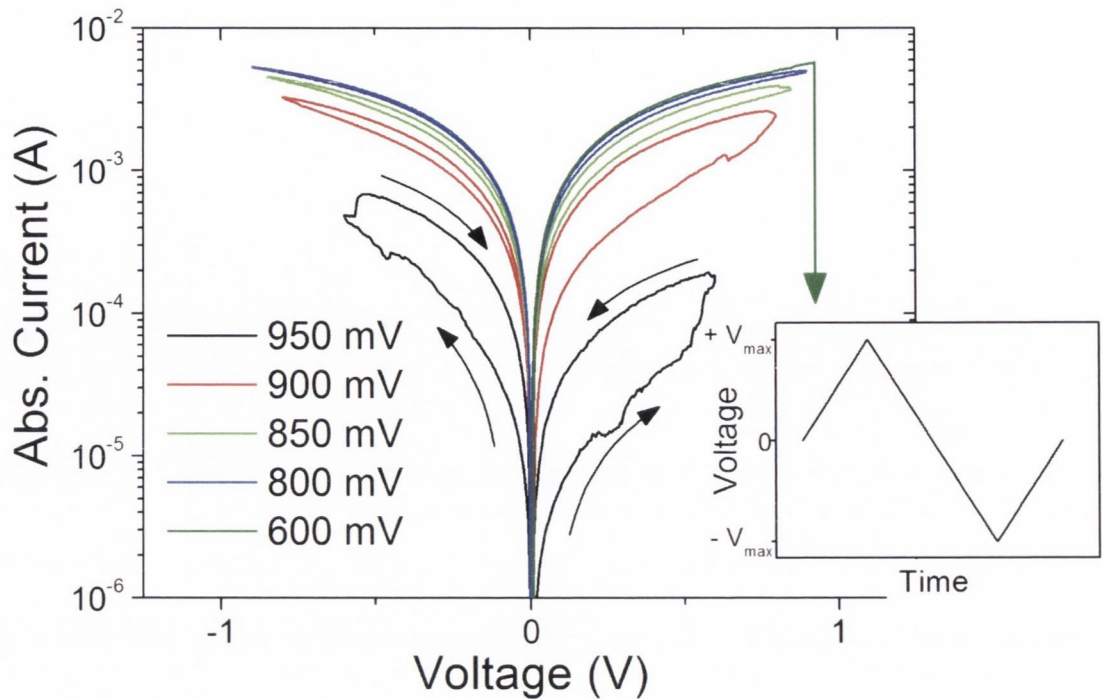
FIGURE 4.9. Network evolution in a $D/L_{NW} = 2.74$ Ag nanowire network. As the voltage across the network is swept, the addition of further activation cells to the conductive path results in a non-linear current response, producing hysteretic I-V traces. Arrows indicate direction of current increase. V_{max} is increased with each subsequent sweep, causing further evolution of the connectivity. Inset: voltage-time trace. Sweep rate is ~ 25 mV/s.

upper limits of $\rho(\nu_B)$. As the network is electrically stressed post-activation, the addition of these activation cells to the main conducting path adds parallel conductive pathways to the network, thereby reducing the resistance of the network. This is manifested in the I-V plot as a non-linear increase in current with applied voltage, producing hysteretic curves. This hypothesis is further strengthened by the observed unipolar nature of the effect. As ν_B is considered by to independent of bias polarity, hysteresis should be observed at both positive and negative bias, with the most prominent effect occurring in the direction of the initial sweep, which is the case.

In chapter 3, it was established that the resistance of a junction may be lowered by driving current through that junction, and that for the case shown mA current levels were required to reach the lowest resistance, though such high currents were not required in all cases. It should then follow that driving current through a network will have a similar effect and enhance the conductance of the junctions, resulting again in hysteretic I-V curves. The hysteresis demonstrated by small, sparse networks near the percolation threshold will then be dominated by junction enhancement, rather than the activation of parallel pathways as these are few in number. However, parallel pathway activation is expected to dominate in larger, denser networks where many potential parallel paths exist. The connectivity in random nanowire networks may thus be manipulated, or evolved, through both the addition
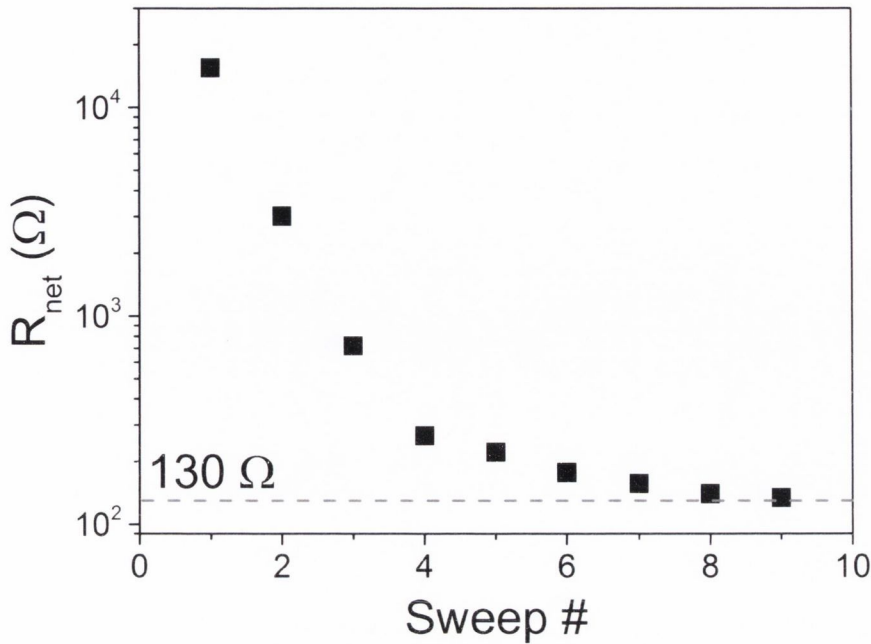
FIGURE 4.10. Evolution of network resistance with sweep number. Data in Figure 4.9 replotted to show the resistance at $|V_{max}|$ for each sweep. The resistance approaches a minimum value of $\sim 130\,\Omega$.

of neighbouring activation cells and the current-driven enhancement of individual junctions. This behaviour has been termed *connectivity evolution*.

The converging hysteresis loops with increasing V_{max} in Figure 4.9 suggest that the network approaches its minimum resistance, where all junctions have been activated and their resistance minimised. Figure 4.10 replots the data in Figure 4.9 to show the network resistance at V_{max} for each sweep, where $+V_{max}$ and $-V_{max}$ are considered as separate sweeps. The resistance of the network asymptotically approaches a value, R_{final}, of approximately $130\,\Omega$. In the context of the connectivity evolution hypothesis this may be explained as a gradual approach toward the minimum junction resistance, assuming a current driven junction enhancement mechanism.

The sudden loss of current at 925 mV is thought to be the result of a hard failure of a nanowire somewhere within the network. Inspection of the network with SEM (Figure 4.8(b)) shows this to be the case. The inset in (b) shows a magnified image of a blown nanowire, presumably a result of the extreme current densities and the resulting Joule heating. In a small, sparse network such as this, the probability for the existence of a bottleneck point, that is, a single nanowire or junction, is quite high. At high currents the current densities through such a bottleneck are then extremely high, and are thus prone to failure. Estimating a diameter of 80 nm, the current density at the point of failure is $\sim 10^{11}\,A\,m^{-2}$. At such extreme current densities, it is unsurprising that a failure occurred. Indeed, the ability of the nanowire to sustain such extreme currents poses some interesting questions regarding the energy dissipation in these nanostructures, which are unfortunately beyond

FIGURE 4.11. Dark field optical microscope image of $D/L_{NW} = 5.48$ network, the edges of which have been cut using a FI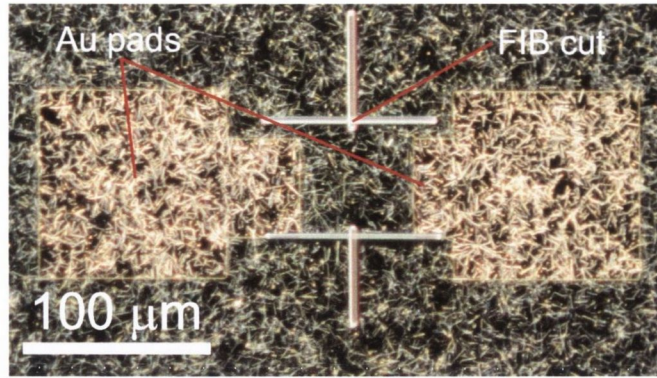B. This is done to prevent contributions to the conductance from outside the network area. In this case, the top edge was missed slightly, and the cut was therefore unsuccessful.

the scope of this work.

4.2.2 SCALING OF CONNECTIVITY EVOLUTION

The results of electrically stressing a small network present some interesting findings regarding the connectivity of random networks, and how this may be affected by an external stimulus. In order to study this behaviour further, the scaling of the phenomenon was investigated. Based on the activation cell theory, it is expected that a far greater number of cells will be present in a larger network, however the vast majority of these are expected to be disconnected from the primary conducting path immediately following activation. It should then be possible to evolve the connectivity within a larger network to a greater degree than for a smaller network.

In order to directly compare the results from separate networks, two network sizes were prepared on the same spray-deposited network, where $T = 75\%$. A $D/L_{NW} = 5.48$ network was prepared via bottom contacting followed by spray deposition, and a $D/L_{NW} = 137$ network was subsequently prepared on the same network by the shadow mask technique. Of these two contacting methods, bottom-contacting is expected to have the highest associated contact resistance due to imperfect connections between the Au pad and the nanowires, however as will be shown, this does not impact the results obtained. One challenge associated with the characterisation of confined networks is that conductive paths may form outside the defined network area, possibly reducing the validity of any arguments made. To prevent external conduction paths contributing to the conductance of the network, the edges of the defined network were cut using a FIB, thereby eliminating any possible contributions from outside the network area. A dark field optical microscope image of one such FIB-cut network is shown in Figure 4.11, where $D/L_{NW} = 5.48$.

Figure 4.12(a) and (b) show the I-V curves for the post-activation electrical stressing behaviour of the $D/L_{NW} = 5.48$ and $D/L_{NW} = 137$ networks, respectively. It is clear that
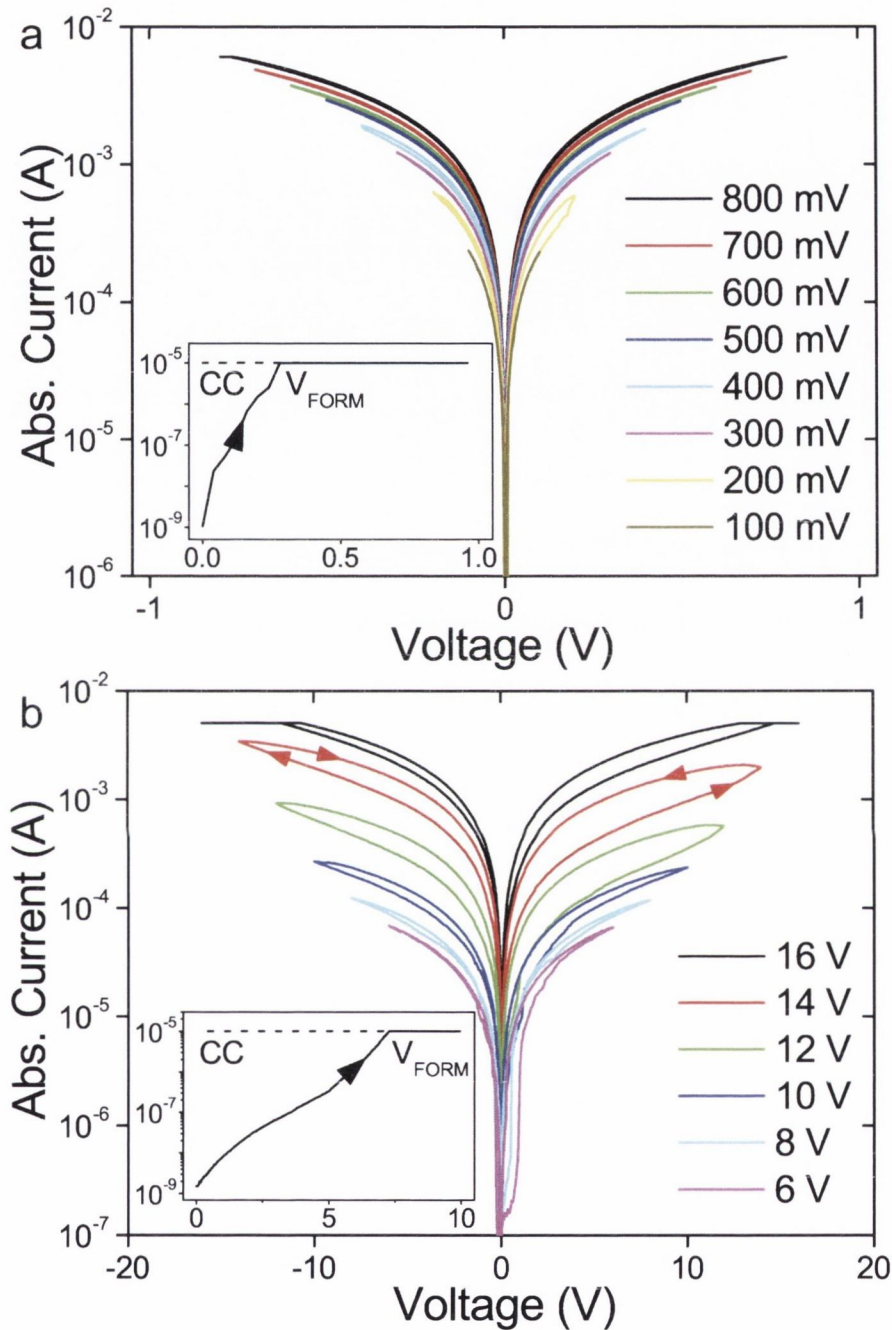
FIGURE 4.12. I-V curves showing hysteresis in $D/L_{NW} = 5.48$ and $D/L_{NW} = 137$ networks fabricated on the same sample, where $T = 75\%$. (a) Relatively small levels of hysteresis are present in I-V sweeps, indicating very small degree of connectivity evolution. Sweep rate was 25 mV s^{-1}. (b) Significantly larger hysteresis loops are present, confirming the hypothesis that large networks have many alternate pathways to conduction that may be activated under electrical stress. Sweep rate was 250 mV s^{-1}. Insets show the forming sweeps in each case.
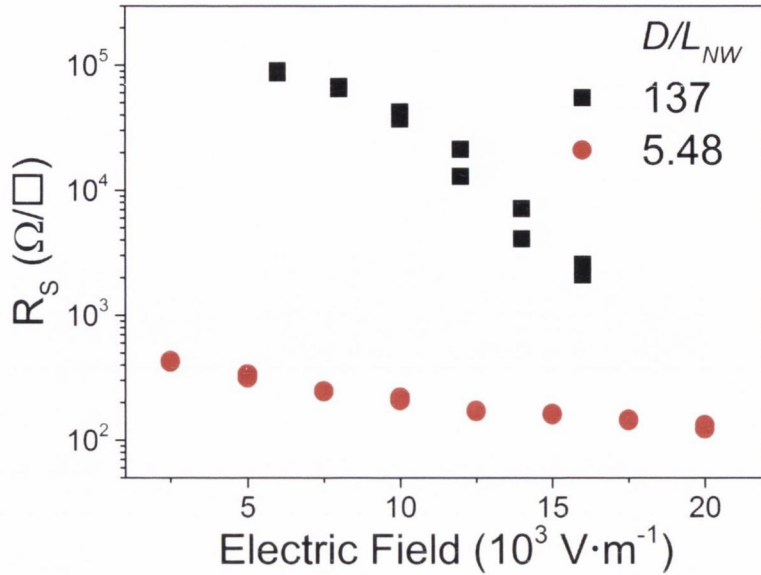
FIGURE 4.13. Network sheet resistance, R_S, as a function of the maximum electric field experienced during each sweep for both $D/L_{NW} = 5.48$ and 137 networks shown in Figure 4.12.

in both cases hysteresis is present in the I-V curves. In these measurements, the current was limited to 7 mA whilst performing voltage sweeps due to the limitations of the electrical characterisation system. The two network sizes evolve connectivity, and therefore change their resistance, to very different degrees. In the case of the smaller, $D/L_{NW} = 5.48$ network, the resistance of the network does not change significantly from the initial sweep to when the current limit of 7 mA is reached. However, the $D/L_{NW} = 137$ network shows a resistance change of over an order of magnitude prior to hitting the current limit.

As the voltages applied in both cases differ significantly, it is far more appropriate to compare the behaviour in terms of electric field. Figure 4.13 re-plots the data in Figure 4.12 and compares the change in sheet resistance as a function of the maximum electric field experienced during each sweep. It is clear that, despite experiencing almost equivalent electric fields, the degree of change in the sheet resistance varies significantly for the two network sizes examined. This result confirms the previous assumption that a large network is capable of significantly higher levels of connectivity evolution, as there are a larger number of parallel pathways available to the network which may be activated under electrical stress.

It is also apparent that neither network shown in Figure 4.12 experiences a failure, as was the case for the $D/L_{NW} = 2.74$ network, despite higher current levels being achieved in both cases. It is hypothesised that this is due to the formation of parallel pathways within the network, reducing the total current through any particular nanowire or junction, and thereby limiting the Joule heating effect. The capacity of a network to evolve connectivity can thus be thought of as a redistribution of the electrical stress through the activation of alternate pathways.

FIGURE 4.14. Electrically stressing Ag nanowire networks to failure. Current and sheet resistance plotted as a function of electric field for (a) $D/L_{NW} = 5.48$, and (b) $D/L_{NW} = 137$ networks.
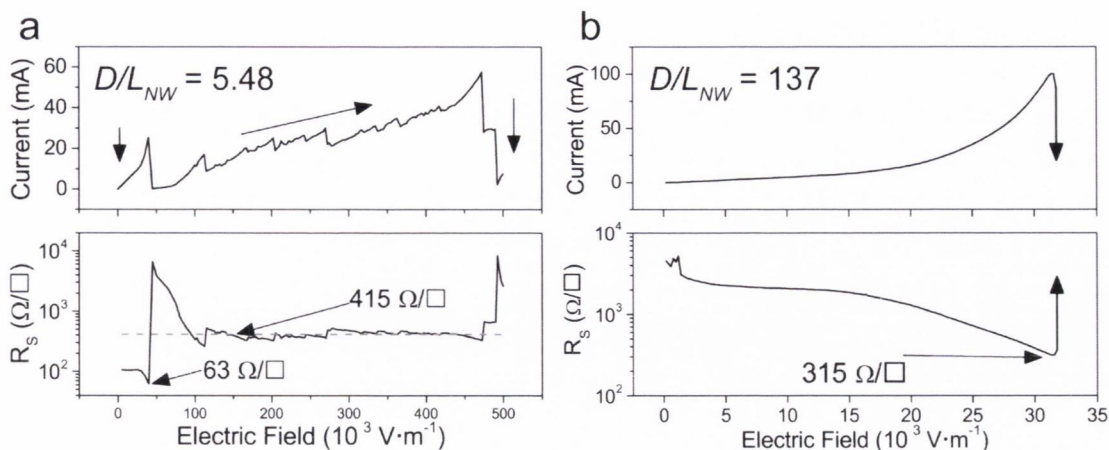
4.2.3 LIMITATIONS OF CONNECTIVITY EVOLUTION

The lack of a clear convergence of the I-V curves in Figure 4.12(b) would suggest that the network connectivity has the capacity to evolve further. To investigate the limits of connectivity evolution, the networks were electrically stressed to the point of failure. For this, a single Keithley SMU was employed to apply a voltage across each network. Use of a single SMU in this way removes the current limitations inherent in the more complex electrical characterisation system (system-I), though current sensitivity is sacrificed as a result. The electrical stress curves, plotting both current and sheet resistance as functions of the applied field, are shown in Figure 4.14 for both $D/L_{NW} = 5.48$ and $D/L_{NW} = 137$ networks. The networks were driven to the point that failure occurred and the resistance rose significantly; the lowest sheet resistance observed was deemed to represent the limit of the connectivity.

The $D/L_{NW} = 5.48$ network reached a minimum sheet resistance of $63\,\Omega/\square$ at an electric field of $40\,kV\,m^{-1}$, however immediately following this the resistance increased suddenly, presumably due to nanowire failure in a critical path. As the applied field increased however, the sheet resistance recovered and remained stable at $415\,\Omega/\square$. The network eventually failed completely under an extremely high field of $500\,kV\,m^{-1}$ while passing a current of 60 mA. The larger $D/L_{NW} = 137$ network reached a minimum sheet resistance of $315\,\Omega/\square$ at a field of $32\,kV\,m^{-1}$ and passing a current of 100 mA, before failing completely. It is interesting to note that both networks reached a minimum sheet resistance at very similar fields: $40\,kV\,m^{-1}$ and $32\,kV\,m^{-1}$ respectively, though it is not clear if this is merely coincidence, or if it reflects limitations inherent to the material.

In order to draw conclusions about the levels of connectivity reached by each of these networks, conditions for complete connectivity must first be established. To do this, a network of equal density ($T = 75\%$) was thermally treated to remove the PVP coating.

The as-sprayed networks were placed in a furnace under N_2 flow for 2 hours at 200 °C. Electrodes were subsequently deposited and sheet resistance measurements performed. It was established in chapter 3 that an annealing step produces very low junction resistances, therefore a similar treatment will result in the highest possible sheet resistance for a given network by optimising the junctions. The performance of the annealed network is then considered to be the benchmark for optimal connectivity. Results of these measurements showed an average 2-probe sheet resistance of $77 \pm 4\,\Omega/\square$ and a 4-probe resistance of $21\,\Omega/\square$. These numbers are approximately an order of magnitude higher than those of state-of-the-art films,[5,6] and this reflects the rather low aspect ratios of the wires used in this study ($L_{NW}/d_{NW} \approx 85$).

Comparing the results of the electrical stressing experiments with these annealed networks, a number of conclusions may be drawn. Firstly, based on these results it appears that the $D/L_{NW} = 5.48$ network achieves approximately complete connectivity, as the measured minimum sheet resistance of $63\,\Omega/\square$ is very close to the $77 \pm 4\,\Omega/\square$ measured for the annealed network. The much larger, $D/L_{NW} = 137$ network however does not appear to achieve complete connectivity, only achieving a minimum sheet resistance approximately four times that of the annealed network, indicating the connectivity was far from complete. This result would indicate that in a large network such as this there remain many nanowires or activation cells that exist too far from the conductive pathway to contribute to the conductance of the network, thereby limiting the extent to which the connectivity may be manipulated. This conclusion is strengthened as the $D/L_{NW} = 5.48$ network was bottom-contacted, and is thus expected to have a higher associated contact resistance compared to that of the larger, top-contacted network.

Figure 4.15 shows the data in Figure 4.13 replotted to include this maximal stress data. It is clear from these results that through controlling the electrical stress, the connectivity, and therefore the conductivity, of various networks may be manipulated and controlled with a high degree of precision; although the direction of this control is limited due to the irreversible nature of the PVP breakdown mechanism. Additionally, the degree to which this may be controlled depends strongly on the network size. By incorporating a non-linear component such as PVP at the nanowire junctions, the behaviour of the network is altered from that of an ohmic conductor to create a material whose resistance is electrically tunable.

4.3 Passive Voltage Contrast Imaging of Ag Nanowire Networks

Passive voltage contrast (PVC) imaging in SEM was introduced in chapter 2 as a technique initially developed to qualitatively analyse a microchip and identify faults such as shorts or opens in a microscopic or nanoscopic circuit. In this section, PVC imaging is used to image networks of Ag nanowires, enabling the visualisation of conductive pathways in random nanowire networks, which supports the arguments made thus far in this chapter. The work presented in this section was performed in collaboration with Dr Jessamyn Fairfield.
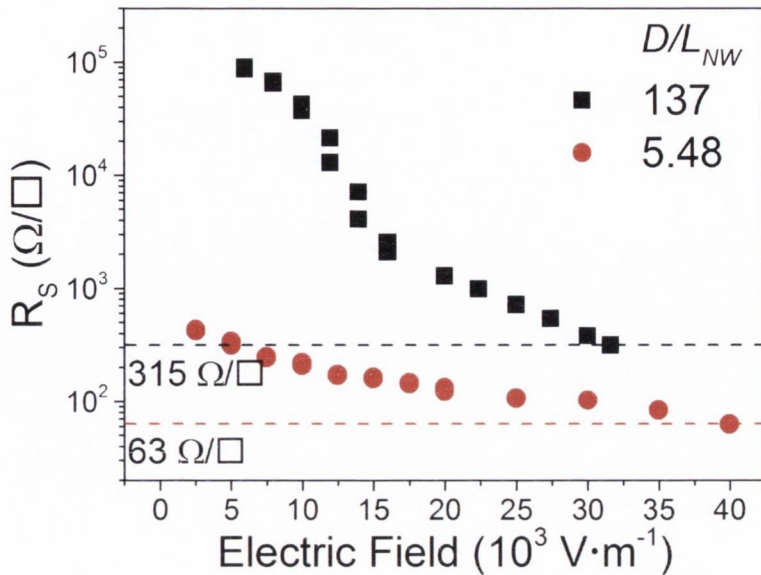
FIGURE 4.15. Re-plot of Figure 4.13 to include maximum stress data. The data shows that the sheet resistance of the film may be controlled with a high degree of accuracy, by controlling the applied electric field. A tunable material such as this is extremely valuable from a technological perspective.

As explained in chapter 2, the conventional mechanism for PVC operation is the generation of a positive charge on a surface due to the incident beam generating a greater number of secondary electrons than impinge the surface for a small range of accelerating voltages (typically 1-2 kV). This positive charge, if not grounded, then impedes the escape of further electrons thereby creating a darkened region in the image. This work employs a different mechanism for contrast generation however, as rather than appearing darkened, floating objects appear as bright regions within the image relative to their surroundings. The mechanism for this contrast is simple electrostatics, as those objects not connected to ground generate a negative charge build up due to electron bombardment. This negative charge results in an enhanced scattering of the incident electrons, creating bright regions in the image. Grounded objects do not build up charge in this way, scattering incident electrons to a smaller degree and thereby generating regions of differing contrast in the image. Figure 4.16(a) schematically illustrates this mechanism. To achieve contrast using this technique, the In-lens detector must be used as it is most sensitive to primary scattered electrons. The differences in SE2 and In-lens signals are highlighted in Figure 4.17, demonstrating the strength of the technique.

A PVC SEM image of a $D/L_{NW} = 4.11$ Ag nanowire network is shown in Figure 4.16(b), demonstrating this contrast mechanism. The Au electrodes are connected to ground by contacting micro-needles, and as such all objects that have an ohmic connection to these electrodes appear darkened relative to floating objects. The network in this image was electrically activated and the connectivity evolved prior to acquiring the image. The PVC image clearly shows a region of darkened nanowires spanning the two electrodes, as well as
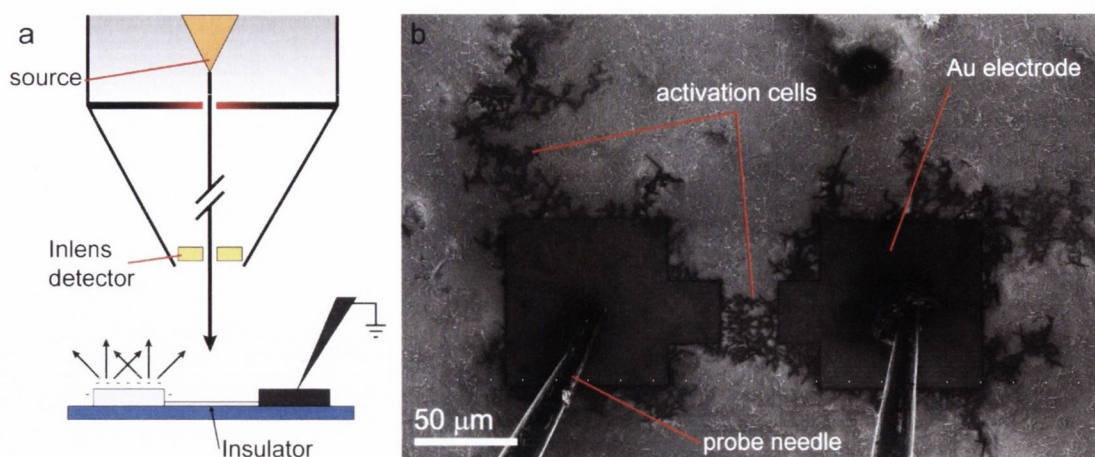
FIGURE 4.16. Passive voltage contrast imaging of activation cells in a Ag nanowire network. (a) Schematic illustration of PVC mechanism. (b) PVC SEM image of an activated $D/L_{NW} = 4.11$ Ag nanowire network. Micro-needles connect both electrodes to ground inducing the PVC mechanism. Activation cells connected to the Au electrodes are clearly visible as darkened regions relative to the rest of the network.

extended regions of darkened wires on all sides of the electrodes. This clearly demonstrates the existence of activation cells, and is consistent with the model developed to explain the results of electrical characterisation, though it should be noted that only those cells that are connected to either electrode are visible. The presence of significant clusters of activated nanowires that lie outside of the network area demonstrates that pathways do not necessarily take the shortest path between electrodes. This also confirms the need to isolate the network area with the use of FIB cuts, as described previously, when performing accurate sheet resistance measurements of small networks such as these, as significant contributions to the conductance may exist far outside the network area.

The PVC imaging technique is a powerful tool, and may be used to verify and expand upon many of the hypotheses presented thus far in this chapter. Figure 4.17 shows both SE2 and Inlens (PVC) SEM images of the $D/L_{NW} = 2.74$ network presented in section 4.2. Viewing the two images side-by-side in this fashion highlights the strength of the PVC technique to clearly distinguish between activated and non-activated nanowires. It was argued in section 4.2 that given the sparsity of the network, the primary mechanism for the connectivity evolution observed in the I-V behaviour (Figure 4.9) was most likely current induced junction enhancement. As the PVC image allows complete visualisation of the conductive pathways, it can be clearly seen that very few nanowires contribute to the conduction of the network. While based on this evidence alone no definitive conclusions can be made, it would appear that the decrease in network resistance (over two orders of magnitude) observed in Figure 4.9 is a result of junction enhancement, rather than due to the activation of parallel pathways.

PVC imaging may also be used to visualise the activation and evolution processes of larger networks. Figure 4.18 shows the electrical activation and evolution of a $D/L_{NW} =$
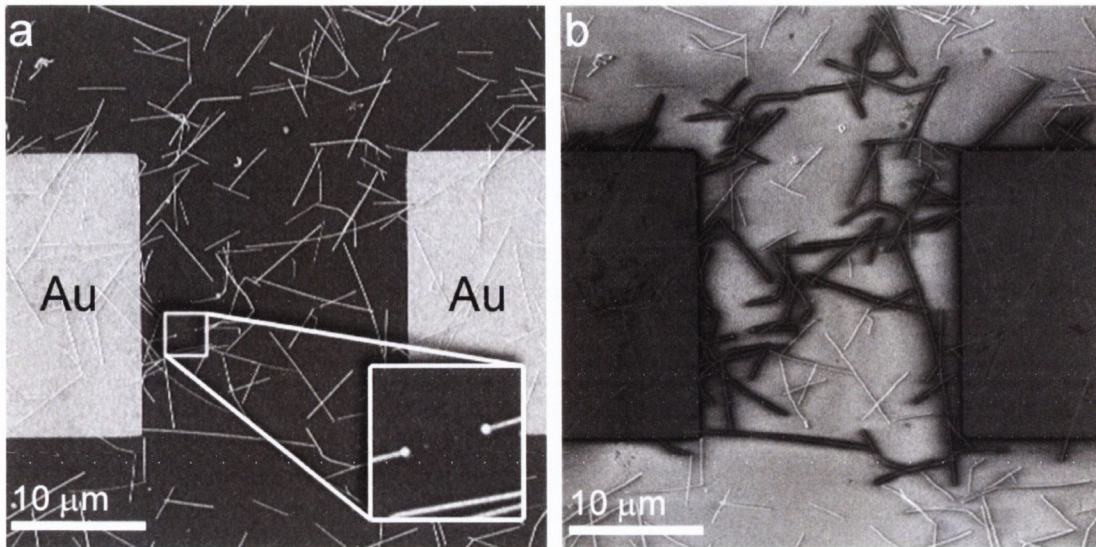
FIGURE 4.17. SE2 (a), and In-lens PVC (b) images of the $D/L_{NW} = 2.74$ network shown in Figure 4.8. PVC imaging clearly highlights those nanowires that are electrically connected to the electrodes which therefore contribute to conduction.

5.74, $T = 85\%$ network visualised in situ using PVC imaging. Prior to imaging, the network was biased with several hundred millivolts in order to stimulate activation cell formation, but prevent complete network activation. Figure 4.18(a) shows the subsequent PVC image. Two large clusters of activated nanowires are visible connected to both left and right electrodes, though they do not overlap. The network was then activated to a compliance current of $10\,\mu A$ and re-imaged, shown in Figure 4.18(b). The formation of a new nanowire activation-cell is visible, spanning the previously disconnected nanowires and completing the conduction path. Finally, the network was stressed beyond activation to force connectivity evolution; Figure 4.18(c) shows the resulting image. An additional activation cell is now visibly connected to the upper portion of the right electrode. These results provide conclusive evidence as to the physical mechanisms underlying the hysteretic I-V behaviour, and verify the connectivity evolution hypothesis.

The passive voltage contrast technique presented in this section provides a novel, yet convenient method to visualise nanowire networks, and in particular to examine the effects of connectivity manipulation through electrical stressing. Use of PVC imaging provides visual evidence for the mechanisms that could previously only be predicted from a theoretical model. While conductive AFM provides a similar ability to visualise the connectivity, it is a notoriously difficult technique to perform on a nanowire network, while also being limited in scan area and speed of image acquisition. The versatility of SEM allows in situ electrical measurements to be performed via the contacting probes, whilst simultaneously imaging the network to observe the corresponding changes in connectivity. In chapter 5, these concepts are drawn upon as a helium ion microscope PVC technique is presented, utilising the unique properties of the ion beam, demonstrating stronger contrast than that presented here, and providing a unique way to control and model connectivity evolution.
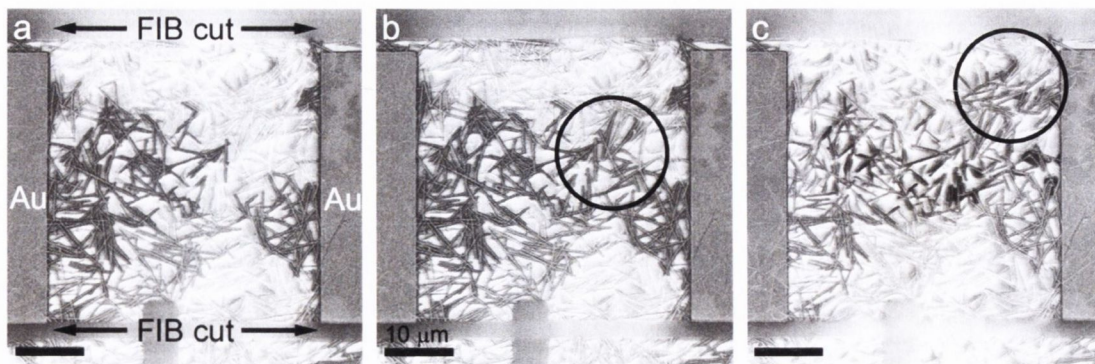
FIGURE 4.18. Visualising activation and connectivity evolution in a Ag nanowire network ($D/L_{NW} = 5.48$; $T = 85\%$). (a) PVC image of a pre-activation network. Activation cells are visibly connected to both left and right electrodes. (b) Upon activation, a new cell of nanowires is visible (circled), completing the conduction path. (c) Formation of a new activated nanowire cell on the right hand electrode (circled) is the result of electrically stressing the network beyond activation, verifying the theory of connectivity evolution through the addition of parallel pathways.

4.4 CONCLUSIONS

In this chapter, the electrical behaviour of PVP-coated Ag nanowire networks was presented. Building upon the results of chapter 3, the scaling of electrical breakdown in Ag nanowire networks was studied using conductive atomic force microscopy. A theoretical model, developed to explain the results of the CAFM study, found that a voltage applied across a network of nanowires, modelled as capacitors with a distribution of breakdown voltages, stimulates the formation of activation cells through a local cascade effect. As the applied voltage is increased, these activation cells overlap eventually forming a conductive pathway between two interrogating electrodes.

The post-activation electrical behaviour of these networks was then examined. Performing voltage sweeps across an activated network resulted in hysteretic I-V curves as the resistance of the network lowered under electrical stress at both positive and negative bias – a phenomenon dubbed connectivity evolution. Based on the previously developed theoretical model, this suggested the addition of activated nanowires to the conduction path. In the case of a very sparse network, where $D/L_{NW} = 2.74$, it was found that the resistance approached a minimum value before failure occurred at high current density. The activated networks were also characterised using a novel passive voltage contrast imaging technique, that allows clear visualisation of the nanowires contributing to the conductive pathway. It was concluded that the connectivity evolution observed was a combination of additional nanowire activation and the current-induced junction enhancement observed in chapter 3.

The post-activation behaviour was compared for two nanowire networks, of equal density, of size $D/L_{NW} = 5.48$ and $D/L_{NW} = 137$ respectively. It was found that through controlling the electric field across a network, the connectivity, and thus the conductivity,

of a network may be arbitrarily increased, and that the degree of control strongly depends upon network size. The limits of connectivity evolution were also investigated by electrically stressing each network to the point of failure. Comparing the lowest sheet resistance obtained with that measured for an annealed network of equal density, it was observed that smaller networks may be driven to achieve complete connectivity, however the degree to which the connectivity may be evolved by an electric field is limited for larger networks.

The results of this chapter are developed upon in chapter 5, where the electrical behaviour of Ni nanowire networks is examined. It was established in chapter 3 that Ni nanowire junctions display reversible resistive switching behaviour, and the addition of this functionality is examined in the context of network evolution.

REFERENCES

[1] NIRMALRAJ, P. N., BELLEW, A. T., BELL, A. P. ET AL., *Nano Letters* **2012**, *12*, 5966–5971.

[2] CHAE, S. C., LEE, J. S., KIM, S. ET AL., *Advanced Materials* **2008**, *20*, 1154–1159.

[3] CHUA, L. O., *Circuit Theory, IEEE Transactions on* **1971**, *18*, 507–519.

[4] STRUKOV, D. B., SNIDER, G. S., STEWART, D. R. ET AL., *Nature* **2008**, *453*, 80–83.

[5] DE, S., HIGGINS, T. M., LYONS, P. E. ET AL., *ACS Nano* **2009**, *3*, 1767–1774.

[6] LANGLEY, D., GIUSTI, G., MAYOUSSE, C. ET AL., *Nanotechnology* **2013**, *24*, 452001.

5

THE EMERGENT PROPERTIES OF Ni NANOWIRE NETWORKS

The evolutionary behaviour exhibited by networks of Ag nanowires is a fascinating phenomenon both from the point of view of understanding connectivity in complex networks and how this may be manipulated, but also from a novel device perspective as the behaviour is analogous to the famed memristor. However, due to the electrical breakdown mechanism of PVP, reversible switching in the Ag-PVP system is not possible at this time. Ni nanowires, as shown in chapter 3, display reversible resistive switching, and are thus an ideal candidate to investigate evolutionary behaviour in a reversible system, and are the focus of this chapter. In order to fully characterise the scaling behaviour of Ni nanowire networks, this chapter begins by studying the activation of Ni nanowire networks as a function of network size and the nanowire dimensions. The behaviour of networks under electrical stress is then examined as a function of network size, and it is shown that the incorporation of a resistive switching element at the junction results in the emergence of distinct behavioural regimes determined by the network size. The work presented in this chapter is published in the journal *Nanoscale*.[1]

5.1 ELECTRICAL ACTIVATION OF Ni NANOWIRE NETWORKS

Before the behaviour of Ni nanowire networks under electrical stress can be studied, those same networks must first be electrically activated. It was established in chapter 3 that the Ni nanowires used in this work have a native NiO passivation layer. Under the action of a sufficiently large bias a conductive filament forms through this oxide, producing an ohmic connection between the Ni core and the contacting electrode. In order to study the electrical activation of Ni nanowire networks, networks were fabricated via spray deposition and contacted with Ni electrodes deposited through a shadow mask. For this study, a new shadow mask design was developed that allowed for the fabrication of networks as small as $10 \times 10 \ \mu m^2$ in area. An image of this mask design is shown in chapter 2, Figure 2.17.
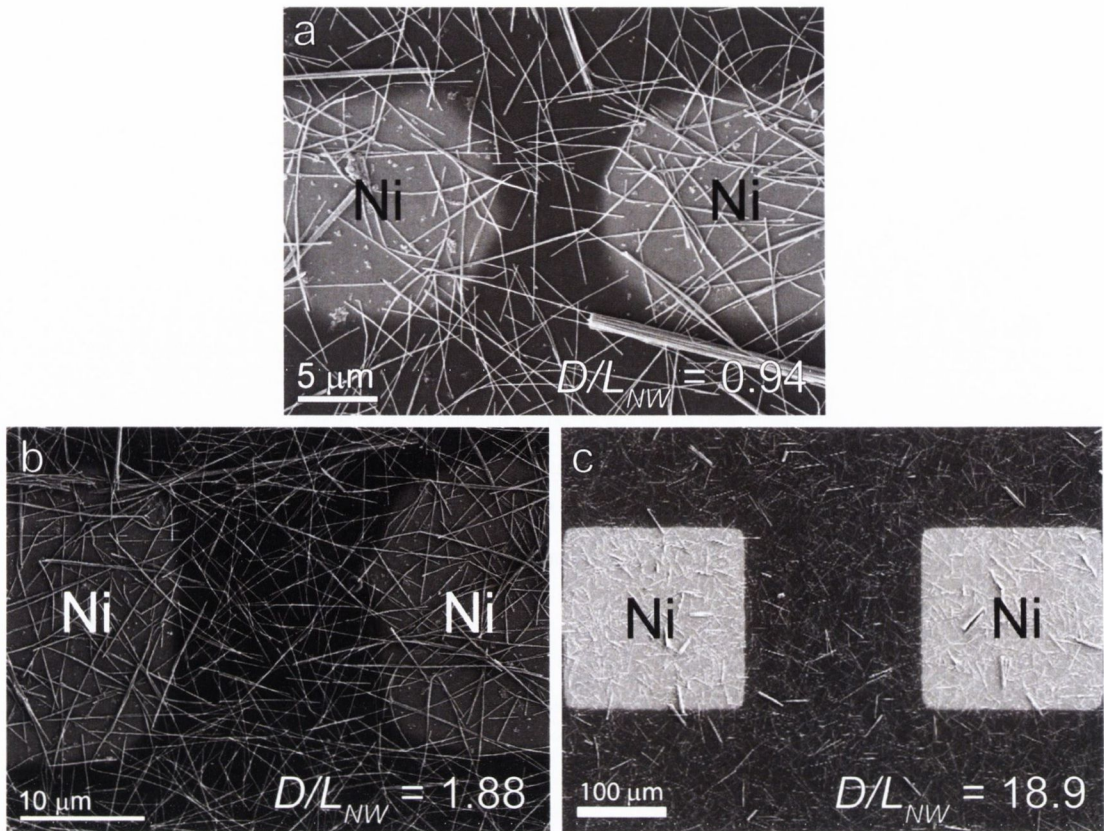
FIGURE 5.1. SEM images of Ni nanowire networks of various sizes: (a) $D/L_{NW} = 0.94$; (b) $D/L_{NW} = 1.88$; and (c) $D/L_{NW} = 18.9$. The nanowires are from batch NB5 in all three cases.

SEM images of various nanowire network sizes fabricated in this manner are included in Figure 5.1.

As was discussed in chapter 3, it was established by Sorel et al. that the sheet resistance of a conducting network may be reduced by increasing the length of the nanowire, and it was postulated that this was due to fewer junctions spanning the electrode width.[2] It is then reasonable to assume that the voltage, V_{FORM}, required to activate or form the network will show a dependence on nanowire length for similar reasons. Similarly, V_{FORM} will depend on the activation voltage per junction, determined by the oxide thickness, t_{ox}. To test this, V_{FORM} was measured for a range of different inter-electrode distances (and hence network sizes) on networks made from three separate batches of nanowires. These three batches, labelled NB3, NB5, and NB7, all demonstrated variations in length and oxide thickness after being extracted from the AAO template. The statistics for these three nanowire batches are detailed in table 5.1. Nanowire diameter and oxide thickness measurements were both made using the TEM, while nanowire length measurements were made using the SEM.

As explained in chapter 3, to form a nanowire junction, or a nanowire network in this case, a voltage is swept across the device until a change of resistance occurs, and a pre-defined compliance current (CC) is reached. A CC of $10\,\mu A$ was used to form all of the

TABLE 5.1. Length, diameter, and oxide thickness statistics of different nanowire batches

Batch	Length (μm)	Diameter (nm)	t_{ox} (nm)
NB3	4.9 ± 3.0	81.5 ± 8.0	7.7 ± 2.1
NB5	10.6 ± 6.7	81.4 ± 6.9	6.0 ± 1.4
NB7	9.6 ± 4.2	87.0 ± 9.3	8.6 ± 3.7

networks demonstrated in this work, as it is the lowest current for which non-volatile memory of the resistance state could be achieved. A plot of V_{FORM} as a function of inter-electrode distance is shown in Figure 5.2(a) for each of the three batches, where approximately the same nanowire density ($T = 82 \pm 3\%$) was used in each case. The data for all three batches of nanowires shown follows a linear relationship, while the slope varies significantly between each. From table 5.1 it is clear that the nanowire length varies from batch to batch, particularly for the batch labelled NB3, which has an average length of only $4.9 \pm 3.0\,\mu m$. Correspondingly NB3 also shows the steepest slope in Figure 5.2. In an attempt to normalise the data, the network size, D/L_{NW}, was plotted against V_{FORM} (Figure 5.2(b)), to take account of the variance in nanowire length. The results from this show that the data from batches NB5 and NB7 now lie on top of one another, while there is still some deviation for batch NB3. Despite this small deviation however, this result indicates that normalising the network size in this manner is appropriate to account for variations in nanowire geometry.

From these plots it is clear that the voltages required to activate Ni nanowire networks are substantially higher than those required to activate Ag nanowire networks of equal sizes; $V_{FORM} = 840\,mV$ for a $D/L_{NW} = 2.74$ Ag network (Figure 4.8). This is due to the much larger energy barrier to conduction presented by the NiO layer, compared to that of PVP. The result of this is that the inter-electrode distance, or network size, available to be activated and thus to be studied, is severely limited by the high voltages required. The electrical
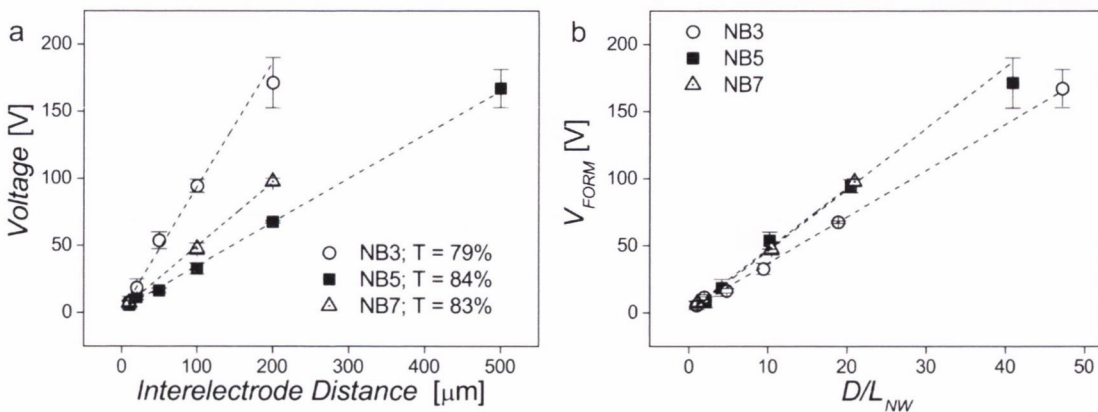

FIGURE 5.2. Forming voltage, V_{FORM}, plotted against (a) inter-electrode distance, D, and (b) the normalised network size, D/L_{NW}.
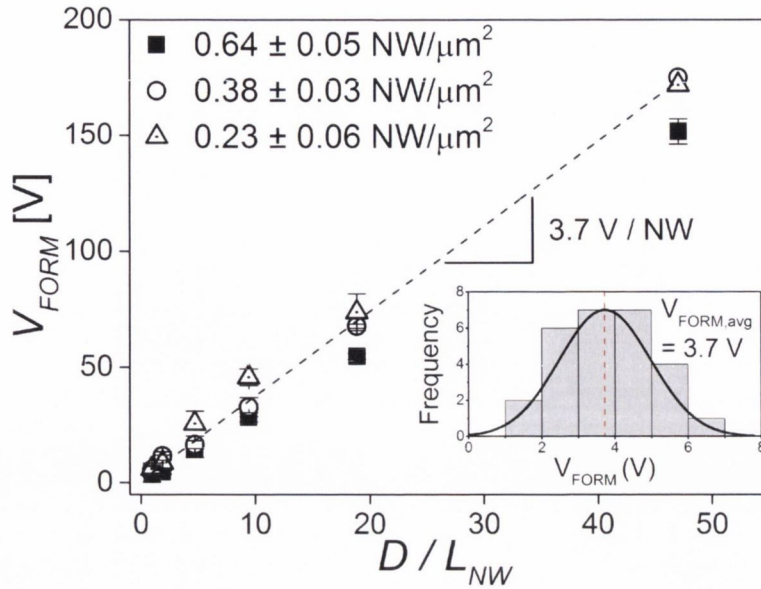
FIGURE 5.3. Scaling of V_{FORM} with network size for different nanowire densities. Data from 0.38 NW μm^{-2} set shows a slope of 3.7 ± 0.1 V/NW Inset: histogram of forming voltages for single Ni nanowires shows a normal distribution, with a mean value of 3.7 ± 1.3 V.

characterisation systems used in this work are limited to ± 210 V, and thus networks of size $D/L_{NW} > 50$ are unavailable for study.

Based on the results shown for Ag nanowire networks in chapter 4, V_{FORM} should show a strong dependency on nanowire density. To test this, networks of different density from a single batch of nanowires, namely NB5, were fabricated and V_{FORM} measured as a function of network size. For each network fabricated, the nanowire density, ρ, and the optical transmittance were both measured. The densities fabricated were $\rho = 0.23 \pm 0.06$, 0.38 ± 0.03, and 0.64 ± 0.05 NW μm^{-2}, corresponding to transmittance values of $T = 84\%$, 78%, and 68% respectively. The results are plotted in Figure 5.3.

From this plot, a weak dependence of the slope on network density can be seen. The slope of this plot, which is the effective breakdown voltage per length of nanowire, should reflect the distribution of breakdown voltages present in the system. At low network density, close to percolation, few pathways are available thereby forcing both weak (small v_B) and strong (large v_B) junctions to be activated in order to create a conductive pathway. At higher network densities however, the conductive path is more likely to form due to the breakdown of primarily weak junctions. Therefore, lower densities will display a slope equal to the average breakdown voltage, while higher densities will show smaller values, which are reflective of the distribution. To test this, V_{FORM} was measured for a range of single Ni nanowires, and the average value was found to be 3.7 ± 1.3 V – this is the voltage required to form an electrical contact between two electrodes contacting a single nanowire, the distribution for which is shown inset in Figure 5.3. The measured slope of the 0.38 NW μm^{-2} data set in Figure 5.3 was 3.7 ± 0.1 V/NW, showing excellent correspondence to that measured for
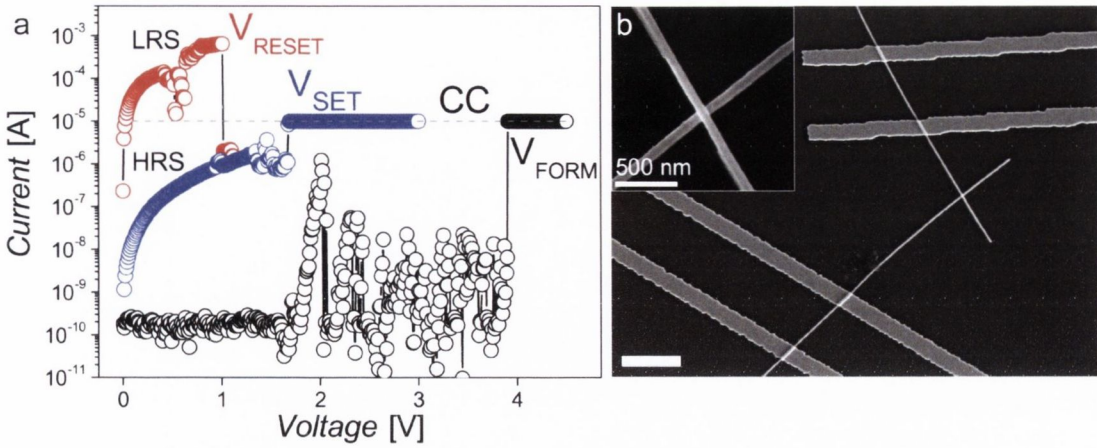
FIGURE 5.4. Resistive switching in a single Ni nanowire junction. (a) I-V curves showing the forming, set and reset steps. (b) SEM image of Ni nanowire junction.

single nanowires. As the network density is increased to $0.64 \pm 0.05 \, \text{NW} \, \mu\text{m}^{-2}$ the slope correspondingly decreased to $3.2 \pm 0.1 \, \text{V/NW}$, reflecting the greater availability of weaker junctions that may be broken down. This then verifies the hypothesis that the distribution of break down voltages, $\rho(v_B)$, is reflected in the slope of a V_{FORM} vs. network size plot.

5.2 RESISTIVE SWITCHING IN Ni NANOWIRE NETWORKS

5.2.1 SMALL NETWORKS: $D/L_{NW} < 2$

Upon establishing a conductive pathway through the network, the behaviour under electrical stress can then be examined as a function of network size. For this, nanowires from batch NB5 were used exclusively to prevent effects arising due to differences in nanowire length or t_{ox}. It was mentioned in chapter 3 that single junctions of Ni nanowires undergo resistive switching (RS) behaviour. This is demonstrated in Figure 5.4 for the junction shown. As discussed in chapter 3, to generate a stable filament through the junction which is held at zero-bias, three forming steps are performed by increasing the compliance current sequentially. The final forming sweep to $10 \, \mu\text{A}$ is shown in Figure 5.4(a, black circles), which is reached at a voltage of 3.91 V. A subsequent sweep confirms the state of the device, that the junction is ohmic and the resistance is $1.4 \, \text{k}\Omega$. By subsequently driving current through the junction in the LRS (Figure 5.4, red circles) the junction is reset as it switches to the HRS ($R = 1 \, \text{M}\Omega$) at a V_{RESET} of 1.01 V and an I_{RESET} of $650 \, \mu\text{A}$. As was discussed in chapter 1, the precise mechanism for filament destruction has yet to be confirmed, however it is widely held that it is induced through Joule heating caused by high current densities in the nanoscale filament. The junction may be switched back to the LRS by sweeping voltage across the device such that the filament forms and the CC is reached at a voltage, V_{SET} (Figure 5.4, blue circles). The voltage required to set the junction is lower than that required to form the device initially, as the filament is not completely destroyed during the
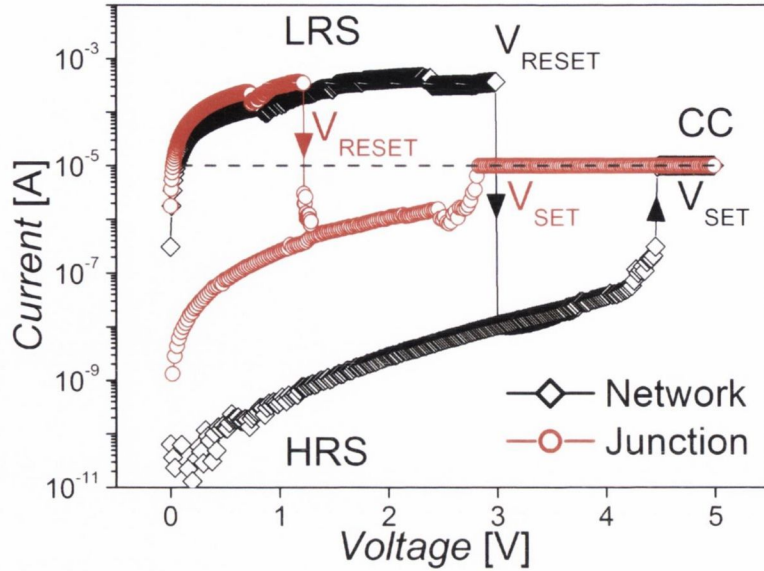
FIGURE 5.5. Resistive switching in a small ($D/L_{NW} = 1.88$) Ni nanowire network. Comparison of resistive switching I-V behaviour of a nanowire network and that of a single junction.

reset process.[3]

It was discovered that electrically stressing a small ($D/L_{NW} < 2$) Ni nanowire network, caused the same resistive switching behaviour to be displayed. This is in contrast to the behaviour observed for small Ag nanowire networks which show evolution of the connectivity, dominated by current-induced junction enhancement. Figure 5.5 shows the resistive switching I-V behaviour of a $D/L_{NW} = 1.88$ network (black diamonds) compared to that of a single junction (red circles). An SEM image of a network similar to this is provided in Figure 5.1(b). The nanowire density for all networks described in this chapter was $\rho = 0.38\,\text{NW}\mu\text{m}^{-2}$, unless otherwise stated. Comparing the nanowire network and single junction, the resistive switching properties remain largely the same. It is well known even for planar devices that there exist large variations in the switching parameters (V_{SET}, V_{RESET}, and I_{RESET}) from device to device, but also within individual devices.[4,5] This remains a major challenge to the widespread implementation of resistive switch-based technology. Given this standard variation in parameters, the differences in V_{SET} seen for a single junction and that of a network are not significant. Additionally, given the difference in path length between a single junction and a conductive network, a higher resistance associated with the LRS of the network compared to that of the junction would be expected. The reset current, I_{RESET}, observed does not appear to vary significantly and in fact is almost identical for both junction and network devices: $348\,\mu\text{A}$ and $366\,\mu\text{A}$, respectively. The implication of this is that a single junction is in fact responsible for the RS behaviour observed in both cases.

Combining what is already understood for Ag nanowire networks with the RS behaviour demonstrated here, a mechanism is proposed to explain the RS behaviour observed in networks, schematically illustrated in Figure 5.6. It was established in chapter 4 that under
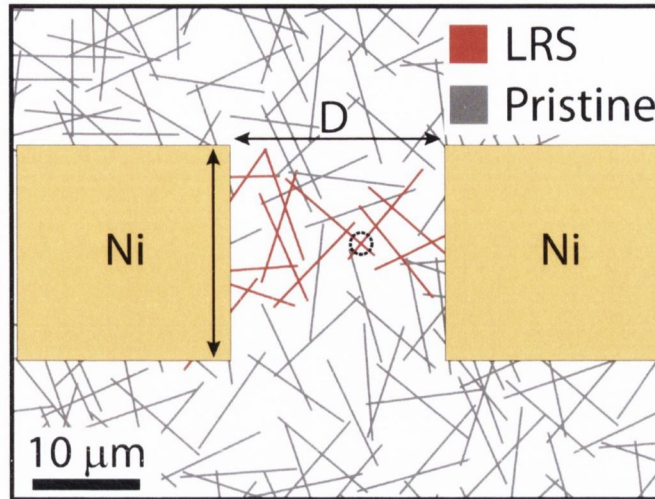
FIGURE 5.6. Schematic of $D/L_{NW} = 2$ nanowire network illustrating the proposed mechanism for RS in networks. An activation cell (red wires) forms, spanning the width of the electrodes, but is reliant upon a single junction (circled). This junction, if stressed, will switch and produce the RS behaviour seen in Figure 5.5

the action of an electric field, cells of activated nanowires form due to a local cascade mechanism (shown as red wires in Figure 5.6). For small networks, such as that described above, it is likely that very few nanowires span the inter-electrode distance. It was found that very small networks of Ag nanowires exhibit catastrophic failure under high currents and this was attributed to the current being forced through a bottle-neck point, creating very high current densities. Translating this same behaviour into a RS system, rather than resulting in a nanowire failure, bottle-neck formation will result in the Joule heating induced dissolution of the conductive filament, switching the junction, and therefore the entire network, to the HRS. This hypothesis is strengthened by the lack of variance in I_{RESET} between both junction and network switches, pointing to the switching of a single junction in both cases.

To demonstrate the fidelity of this RS behaviour over many cycles, a plot of HRS and LRS current as a function of switching cycle is shown in Figure 5.7, for a read voltage of 1.5 V. It is clear that the RS behaviour of this network device is extremely well defined, and exhibits very high ON/OFF current ratios of $\sim 10^5$. The ON/OFF ratio of any RS device is controlled by the device cross-sectional area which determines the leakage current in the HRS. For a network, this area is defined by the two crossed nanowires that undergo RS. It is proposed that the nanoscale nature of this contact leads to minimal leakage current, and thus is responsible for the exceptionally high ratios seen in this network device. While no definitive conclusions can be made at this point, the high fidelity of the current levels in the LRS indicates that the same set of junctions are involved in establishing the LRS, hence the properties of the conductive filaments involved do not vary significantly between cycles. The small variation seen may simply be accounted for by the known variation in the LRS from cycle to cycle, as it was already shown in chapter 3 that the LRS resistance associated with a single junction does indeed vary between cycles. The observed variation in current
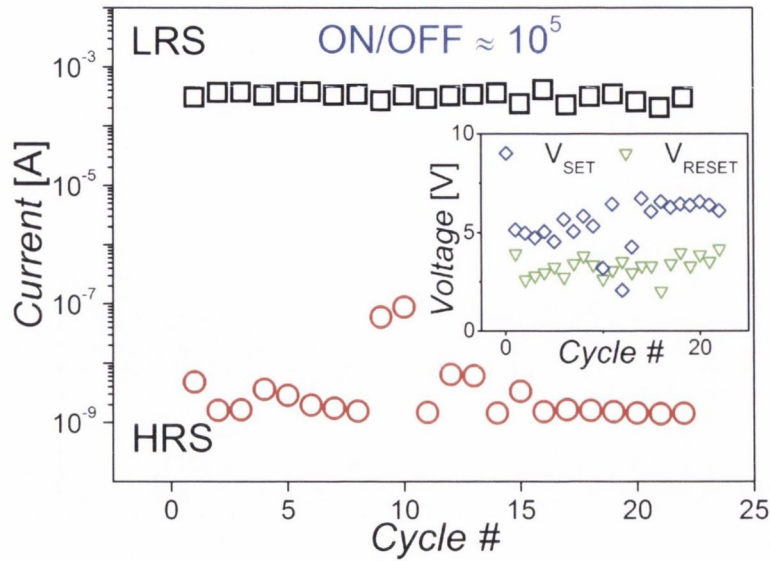
FIGURE 5.7. ON/OFF current ratio for a nanowire network resistive switch. A ratio of 10^5 is demonstrated for over 20 cycles of the nanowire network RS (read voltage = 1.5 V). Inset: V_{SET} and V_{RESET} values for the device as a function of cycle number.

levels in the HRS of almost two orders of magnitude confirms the large variance of the HRS seen by others, as the degree to which the filament is destroyed varies from cycle to cycle. The inset in Figure 5.7 shows the V_{SET} and V_{RESET} values for this same network device, exhibiting tight clustering of the parameters that improves as the device is cycled.

5.2.2 RESISTIVE SWITCHING & PROBABILITY IN NETWORKS ($D/L_{NW} < 10$)

The RS behaviour demonstrated above for a $D/L_{NW} = 1.88$ network is also seen in networks as large as $D/L_{NW} = 9.43$. Figure 5.8 compares the RS operation parameters V_{RESET}, I_{RESET}, and V_{SET} for a number of devices at a range of network sizes alongside those of a single junction ($D/L_{NW} = 0$). To collect this data, each device was cycled a minimum of 10 times, and these data points therefore represent the mean value of each parameter for that device, while the error bars are generated from the standard deviation of values for that device. Both V_{RESET} and V_{SET} show a dependence on network size, consistent with the larger applied voltage necessary to create the required voltage drop across the individual junctions that comprise the switching network. These voltage levels are much smaller than those required to form the initial conducting pathway, consistent with the hypothesis that the vast majority of nanowires remain unaffected by the switching event. The voltage drop is then largely across the switching junction, with only a small contribution falling across the rest of the network. The spread in values observed, while large, is of a similar magnitude to that seen for single junctions, demonstrating once again the inherent variability of RS devices. This is likely compounded in this case by variation in the junction interface caused by inconsistencies in the oxide thickness. It is interesting to note a larger spread in V_{SET}

than that observed for V_{RESET}, again reflecting the variance of the HRS.

For larger networks to display RS behaviour, it must be concluded that single junctions are once again the source of the behaviour. This is in stark contrast to the evolutionary behaviour exhibited by Ag networks of similar size and density. These conclusions are confirmed by the observed independence of I_{RESET} on network size, as shown in Figure 5.8. In the absence of parallel paths, the failure of a single junction is sufficient to switch the network from the LRS to the HRS. Since these junctions are essentially in series this precludes the resetting of multiple junctions along the path, hence the near constant I_{RESET} levels shown. In the context of the connectivity evolution argument presented in chapter 4, breakdown voltages are considerably higher for Ni junctions, therefore the network is unable to create the additional pathways necessary for connectivity evolution below V_{RESET}. To relieve the electrical stress, the critical junction resets and the network is switched into the HRS. Therefore, even for larger networks where evolution through the addition of parallel paths was observed in Ag nanowire networks, RS dominates the behaviour in Ni nanowire networks.

It was demonstrated in chapter 4 that the degree to which a network may evolve increases with increasing network size, as the number of available parallel paths increases. In Ni nanowire networks, this phenomenon manifests itself as a decreasing tendency toward RS behaviour with increasing network size. In larger Ni networks there are significant numbers of junctions that are not connected to the conducting paths within the network, and the network responds to the increasing levels of electrical stress by connecting these junctions rather than causing junctions within the conducting path to undergo RS. This behaviour reflects the intrinsic level of redundancy that exists in larger networks and becomes more pronounced at higher NW densities. This is illustrated in Figure 5.9 where the probability of switching, P_{RS}, is plotted as a function of network size. The RS probability is defined as:

$$P_{RS} = \frac{n(RS)}{n(T)} \tag{5.1}$$

where $n(RS)$ is the number of samples where RS was observed, and $n(T)$ is the total number of samples measured. A device is defined as being capable of RS if it demonstrates at least two complete RS cycles, i.e. LRS $\rightarrow$ HRS $\rightarrow$ LRS $\rightarrow$ HRS, and the RS parameters fall in the ranges set out in Figure 5.8. This definition is not meant to be compared with the state-of-the-art, but rather is a means to categorize behaviour within these network systems.

The initial conducting path (LRS) that is established following the formation process is essentially a percolative connectivity path that spans the network between the two electrodes. When $D/L_{NW} \approx 1$ the majority of the junctions between the electrodes participate in the percolative pathway, so when the network is electrically stressed there is a strong tendency to undergo RS. The failure of a single junction within the percolative connectivity path causes the network to switch to the HRS. However, in the case of a large network ($D/L_{NW} \gg 1$) there remain within the area of network defined by the electrodes many junctions that are not connected to the conducting path. Under electrical stressing these
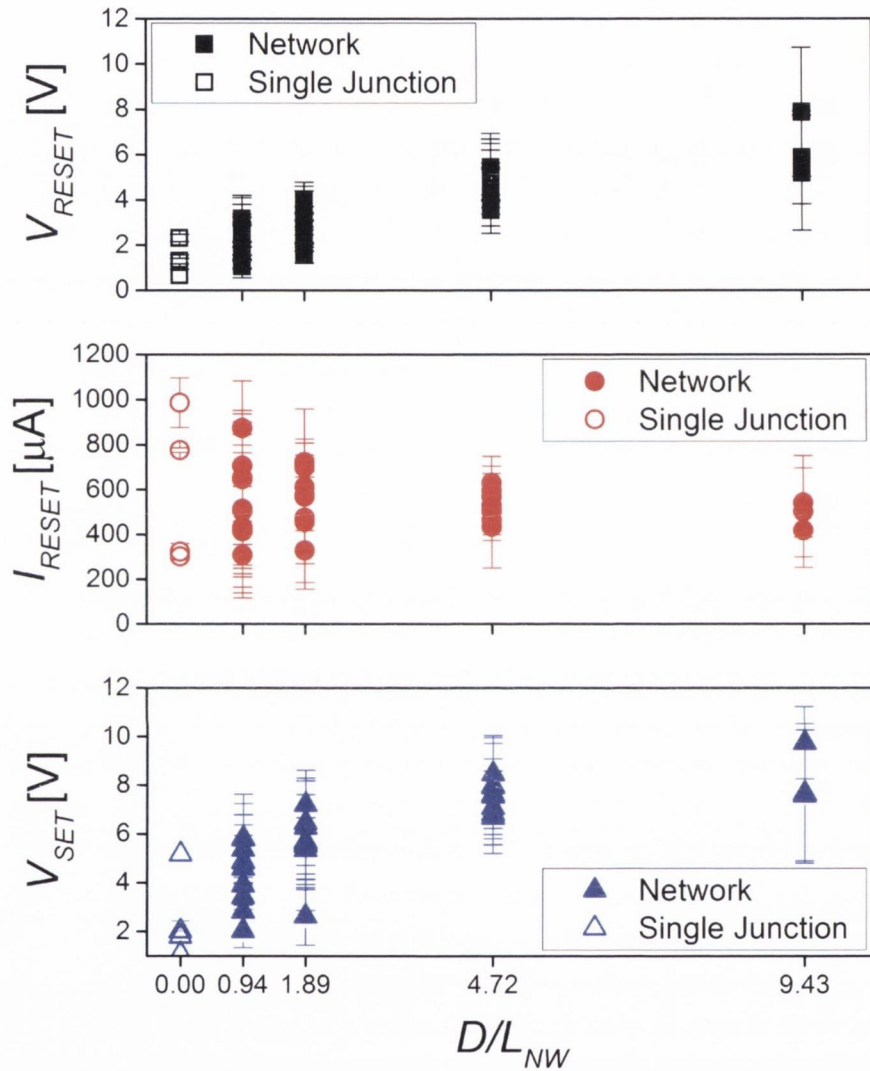
FIGURE 5.8. Scaling of RS parameters V_{RESET}, I_{RESET}, and V_{SET} as a function of network size. Data from multiple devices at various network sizes, where each data point represents the mean value of a device (typically cycled $\sim$ 10 times), while the error bars are generated from the standard deviation. Values for single junctions are also shown ($D/L_{NW} = 0$). A clear dependence on network size is apparent for both V_{RESET} and V_{SET}, but not for I_{RESET}. Given the similar values of I_{RESET} shown for single junctions and all network sizes, it may be concluded that a single junction is responsible for the switching seen in each case. Voltage sweep rates were $\sim$ 50 mV s^{-1}.
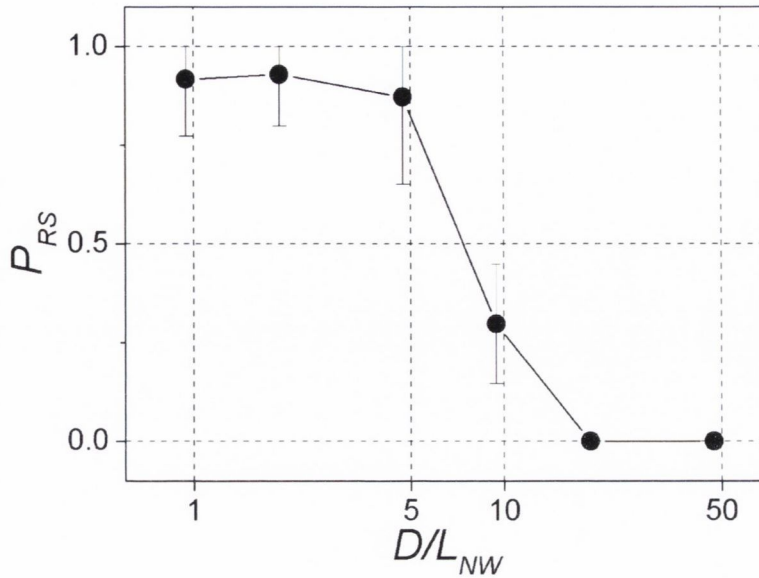
FIGURE 5.9. Plot of switching probability, P_{RS}, against network size, D/L_{NW} (log scale). A sharp decrease in switching probability is seen at $D/L_{NW} = 4.7$. Beyond this point, the capacity of the network to increase the connectivity begins to outweigh the tendency towards RS behaviour. Voltage sweep rate was $\sim 50\,\mathrm{mV\,s^{-1}}$ for all data.

networks tend to add additional junctions to the connectivity path, thereby densifying the conducting pathway within the network. Consequently, the failure of any one junction within this path has an increasingly reduced probability of causing the network to switch between the LRS and HRS, consistent with the data in Figure 5.9. As the evolutionary capacity of a network is dependent upon network density, it is predicted that the network size for which $P_{RS} < 0.5$ will shift to smaller values as network density increases. This is due to an increasing number of parallel pathways available to redistribute the electrical stress resulting in a reduced switching probability.

The plot in Figure 5.9 shows an intriguing result, which is that a random nanowire network demonstrates two distinct behavioural regimes defined by the size of the network addressed. It should be noted that none of the networks measured in this chapter were cut using a FIB, and are therefore effectively infinite in size outside the area of the defined electrodes. Despite this however, controllable behaviour emerges, which is a direct result of the incorporation of a resistive switching element into the nanowire junction. The following section examines more closely the behaviour of larger networks, exhibiting non-RS behaviour.

5.3 BEHAVIOUR OF LARGE NETWORKS ($D/L_{NW} > 10$)

As the network is made even larger, the formation of parallel pathways, either during the electroforming step, or under the action of an applied bias post-activation, becomes increasingly more likely. In the presence of parallel paths, the probability of resistive switching
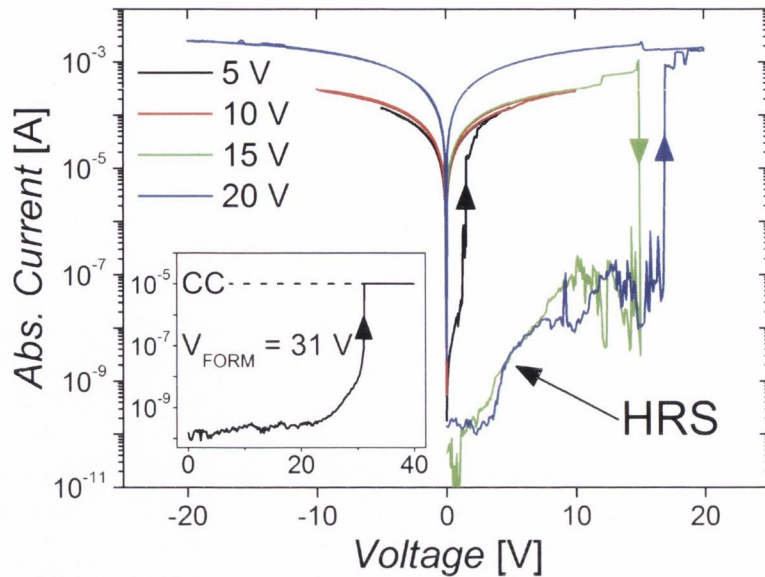
FIGURE 5.10. RS and connectivity evolution behaviour in a $D/L_{NW} = 9.43$ Ni nanowire network. Transitionary network sizes, where $0 < P_{RS} < 1$, may evolve their connectivity through the addition of nanowires to existing conducting paths, indicated by hysteretic behaviour in the I-V curves (see black trace). As P_{RS} is non-zero at this network size, RS behaviour may still be observed; the network switches from a LRS to a HRS as a critical junction is reset (green trace). A subsequent sweep recovers the LRS (blue trace), and the network evolves even further to a resistance of 5.6 kΩ. Voltage sweep rates ranged from 125 mV s^{-1} at 5 V, to 500 mV s^{-1} at 20 V.

behaviour being observed drops to zero, as there are no longer any "critical junctions" acting as a bottle-neck point. Additionally, parallel paths distribute the current load, reducing the current density, and hence the magnitude of the Joule heating effect in the junctions. Thus it is possible to drive higher electric fields across a network, which may result in the addition of further parallel paths, and a reduction in the current load even further. Figure 5.10 shows the I-V traces of sequential voltage sweeps on a $D/L_{NW} = 9.43$ network, where the sweeps followed the sequence $0\,V \rightarrow +V_{max} \rightarrow 0\,V \rightarrow -V_{max} \rightarrow 0\,V$. As the voltage is swept, hysteresis in the I-V curves is apparent, demonstrating the effect of addition of parallel paths.

For a network of this size, while P_{RS} is significantly less than unity it remains finite, as seen in the green trace in Figure 5.10. The network is seen to suddenly jump to a HRS at an I_{RESET} of 1.1 mA. It is proposed that at this point, the voltage required to evolve the network further was greater than that required to reset the weakest junction in the dominant conducting path. This, however, is a reversible phenomenon as can be seen in the subsequent I-V sweep. The network switched back to a LRS at 17 V (blue trace), much lower than V_{FORM}, indicating the re-establishment of a previous conducting path rather than the formation of a new one, which is consistent with the earlier conclusion that the vast majority of the conducting path remains unaffected by prior switching event. Following the re-establishment of the LRS, the network was stressed further to a V_{max} of ±20 V, and was
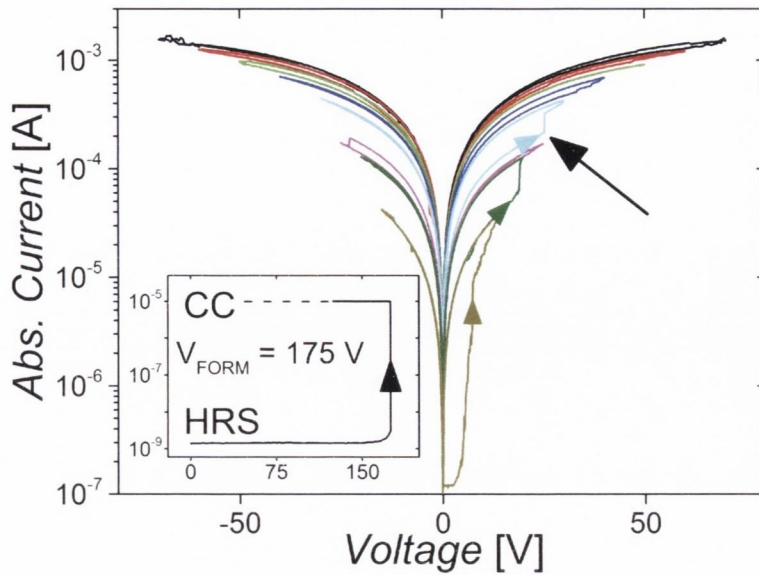
FIGURE 5.11. Hysteretic nature of very large $(D/L_{NW} = 47.17)$ networks. Very large networks provide numerous pathways to current flow, such that the connectivity may be evolved with a high degree of control and the resistance is tunable over a wide range. Sudden increases in current (see arrow) demonstrate the addition of pathways as the voltage is increased. Sweep rates ranged from 25 mV s^{-1} at 5 V to 250 mV s^{-1} at 100 V.

able to evolve connectivity to reach a final resistance of 5.6 kΩ.

Finally, at voltages below V_{max} the current shows exceptional stability, demonstrating that once a network has expanded the connectivity and achieved a new resistance level, this state is stable under current stressing, even at mA level currents. Again, this is expected to be due to the multiple paths over which the network may distribute the current load, creating a behaviour more akin to that of a simple, ohmic material than a non-linear device. Networks of this size then, lying within the transitional region between $P_{RS} = 1$ and $P_{RS} = 0$, display a hybrid behaviour of both regions. While connectivity evolution through the addition of activation cells may occur producing material-like properties, there is still a finite probability that the network may switch to a HRS under high stress.

The electrical characteristics of a very large network $(D/L_{NW} = 47.17)$ were also examined, where $V_{FORM} = 175$ V – close to the limits of the applicable voltage (see Figure 5.3), and thus this represents the upper limit of measurable network sizes. As can be seen from Figure 5.9, the switching probability falls to zero in this range, indicating that behaviour purely controlled by connectivity evolution should be observed. Figure 5.11 shows the I-V curves from sequential voltage sweeps with increasing V_{max}. It is clear that the hysteresis displayed by this network is far more pronounced than that shown in Figure 5.10, allowing precise control over the resistance, and mirroring that seen for large Ag nanowire networks.

One unique feature of Ni nanowire networks are the sudden jumps in current observed, an example of which is highlighted by the arrow in Figure 5.11. This is in comparison to the rather smooth hysteretic loops observed for Ag networks. This is indicative of the
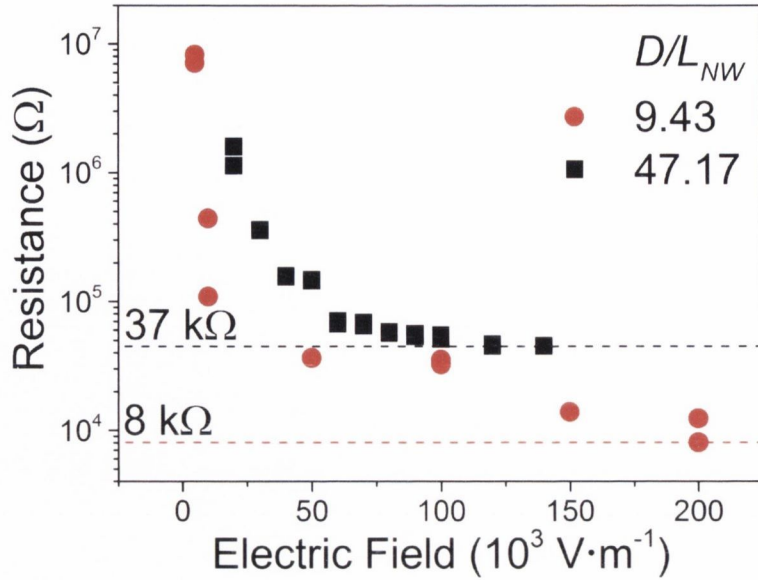
FIGURE 5.12. Plot of network resistance as a function of electric field demonstrating connectivity evolution in $D/L_{NW} = 9.43$ and 47.17 networks. Due to the far greater number of junctions available in the larger network, the connectivity, and hence the network resistance, may be controlled with a greater level of precision. However, the ultimate level of connectivity, and thus the minimum resistance, is achieved for the smaller network, with fewer junctions to be activated. These results are consistent with those observed for Ag networks.

discrete addition of conductive paths, each with a well defined resistance. It is known for Ag networks that connectivity evolution is a result of contributions from activation cell addition as well as current-induced junction enhancement, which may account for the continuous reduction in resistance observed. Current induced enhancement has not been observed for Ni junctions as moderate-to-high current densities cause the junction to reset rather than improve the contact, thus the minimum resistance of an activation cell is defined prior to becoming connected to the main path and passing any appreciable current. It may also be seen that the jumps in current occur at voltages equal to or above the previous value of V_{max}, again a clear indication of connectivity evolution through the addition of parallel conducting channels. The larger hysteresis loops observed at positive bias are a result of the sweep direction, and are consistent with unipolar RS being dependent upon the magnitude, but not the direction of the applied bias.

The connectivity evolution behaviour exhibited by large Ni nanowire networks, as in the case of Ag networks, suggests a material with a tunable resistance. To illustrate the tunability of the connectivity, and to examine the effect of network size on this tunability, the network resistance was plotted as a function of electric field for both $D/L_{NW} = 9.43$ and $D/L_{NW} = 47.17$ networks discussed already, shown in Figure 5.12. From this plot it would appear that the minimum resistance achievable scales with network size, consistent with the results from chapter 4 which show a similar dependence of the maximum connectivity with
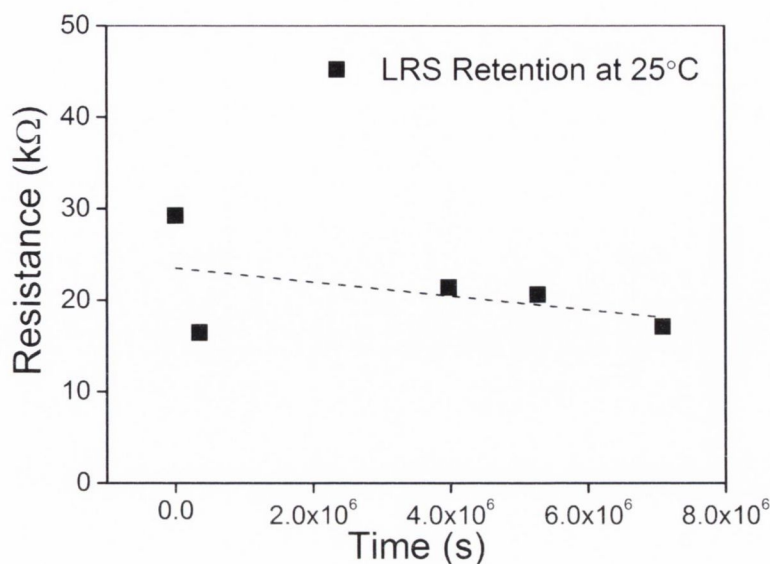
FIGURE 5.13. Resistance – time measurements demonstrating the stability of Ni nanowire networks. An evolved nanowire network, with an initial resistance of 29 kΩ, was measured at different times over an 80 day test period while the sample was left open to atmosphere. No loss of conductivity was observed over the test period, demonstrating good resistance to oxidation.

network size. It is also clear that there is a greater control over the network conductivity for the larger, $D/L_{NW} = 47.17$ network. This greater level of control is again consistent with the results from chapter 4, as the number of available junctions and activation cells scales with D^2, resulting in smaller, discrete steps in the conductance of the network.

For the analysis of Ag networks in chapter 4, the sheet resistance of maximally evolved networks was compared with those that had been thermally treated in order to assess the levels of connectivity achievable through electrical means alone. Unfortunately a similar analysis is not possible for Ni nanowire networks, as there is at present no known method to create a fully connected and conductive Ni nanowire network. This presents a significant barrier to any implementation of this material, and work is currently under way to try to overcome this limitation. Additionally, the extreme electric fields required to push large Ni nanowire networks to maximal connectivity damage the contacting metal electrodes. At electric fields greater than 200 kV m^{-1}, the Ni contact electrodes began to degrade such that often ohmic contact was no longer assured, and thus the results of any stress measurements would be in question, thereby preventing any comparison with a fully optimized network.

As discussed in chapter 3, there is a strong motivation to investigate the properties of Ni nanowire networks due to the formation of the self-limiting NiO layer on the surface of the nanowires, which presents an interesting alternative to other approaches at developing oxidation resistant transparent conductors. To test the stability of an evolved Ni nanowire network over time, a resistance measurement was performed on a $D/L_{NW} = 9.43$ network at different times over a total period of 80 days while the sample was left open to atmosphere,
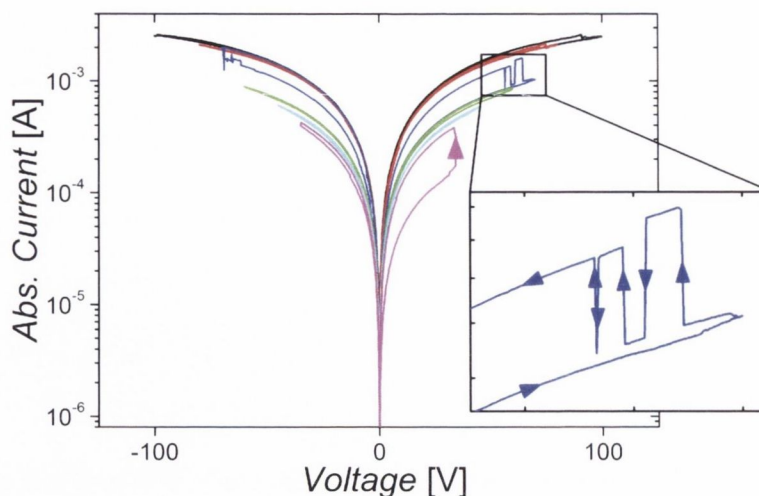
FIGURE 5.14. Adaptive nature of connectivity in large ($D/L_{NW} = 47.17$) networks. Enlarged portion of I-V curve (blue trace) demonstrates the modest effect of individual switching events on the conductivity of the network, illustrating the level of redundancy present in such large networks.

the results of which are shown in Figure 5.13. It is clear that the resistance of the network does not increase over the test period but in fact shows a slight decrease, averaging ~ 20 kΩ as time increased. This demonstrates that, despite each junction consisting of a nanoscale conductive filament, no loss of conductivity is observed and these nanowire networks thus show a good resistance to degradation. This is consistent with retention studies performed on planar NiO RS devices, which show excellent data retention greater than 10^6 seconds at 125 °C.[6]

A large Ni nanowire network therefore demonstrates the properties of an evolutionary material, displaying excellent stability under current loads, and exhibiting good resistance to degradation over time. Thus far the effect of the RS properties of the junctions on the properties of a very large network ($D/L_{NW} \approx 50$) have not been considered, as the level of connectivity is such that it is not possible to switch the network to a HRS, even under high applied voltages. Localised RS within the network may still occur, but the resulting changes in network connectivity induced by these events result in only a modest and temporary reduction in conductivity. The inherent redundancy within these large networks enables them to spontaneously program or reconfigure by activating alternate connectivity pathways or reactivating junctions that had previously been reset. An enlarged view of an I-V curve is shown in Figure 5.14 which demonstrates this behaviour. The conductance of the network rises sharply, only to fall again moments later. This behaviour continues until a stable resistance state is achieved, illustrating a dynamic reconfigurability of the network connectivity under electrical stress.

The scaling phenomena governing the properties of nanowire networks produces two behavioural regimes upon incorporation of RS elements to the nanowire junctions. Larger networks, such as those described in this section, display a connectivity evolution response
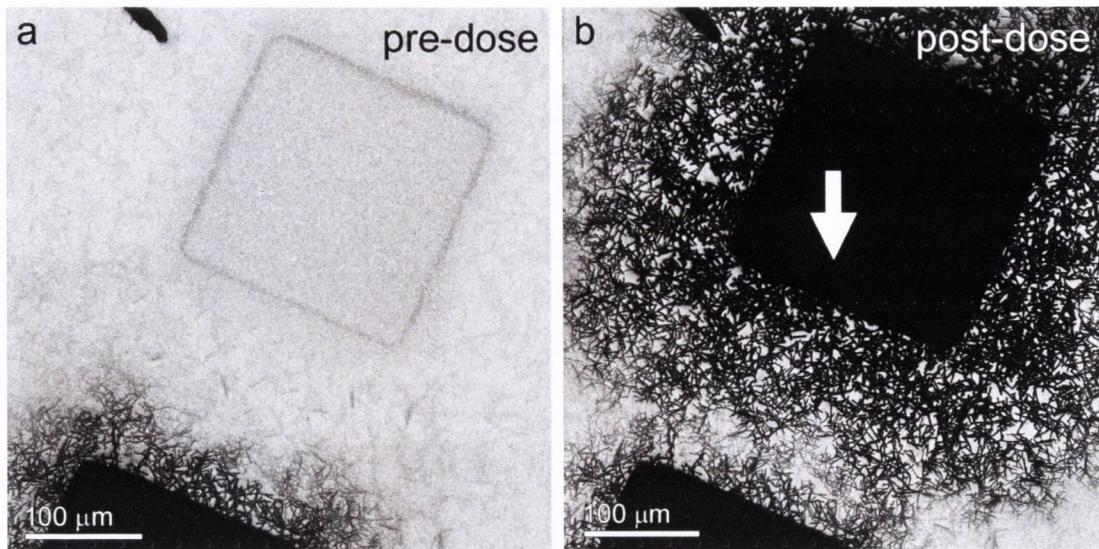
FIGURE 5.15. Helium ion microscope passive voltage contrast images of a Ni nanowire network. (a) Pre-dose, the nanowire network and square electrode (top) show no contrast. (b) By dosing the electrode with He ions (dosing point indicated with arrow) the positive charge distributes to all electrically connected objects, impeding the escape of secondary electrons and producing an extremely strong contrast mechanism in the secondary electron image. A halo of connected nanowires is visible around the electrode, demonstrating the capability of this technique to map connectivity.

to electrical stress that produces materials with tunable resistance that are resistant to degradation over long periods. In addition to this, RS behaviour produces an adaptive behaviour in larger networks where the network dynamically reconfigures the conductive paths in response to high stress. The following section explores the use of a novel helium ion imaging technique to investigate the properties of network connectivity further.

5.4 HELIUM ION PVC IMAGING OF Ni NANOWIRE NETWORKS

A passive voltage contrast imaging technique, based on the helium ion microscope, was introduced in chapter 2. By bombarding a metal electrode with He ions, a positive charge is built up which impedes the escape of secondary electrons, generating a very strong contrast in the SE image. This charge is distributed across all objects that are connected to the electrode through a low resistance, thereby generating contrast in these objects also. Figure 5.15 shows the HIM PVP contrast generated upon dosing a $200 \times 200 \mu m$ square electrode contacting a Ni nanowire network with He ions. Prior to dosing, the electrode and underlying nanowire network show no contrast; the electrode at the bottom of the image was previously dosed and therefore does show contrast. Upon dosing however, a large halo of connected nanowires is visible. In this section, this novel PVC technique is used to visualise and map the connectivity in Ni nanowire networks. This work was carried out in collaboration with Dr Alan Bell.
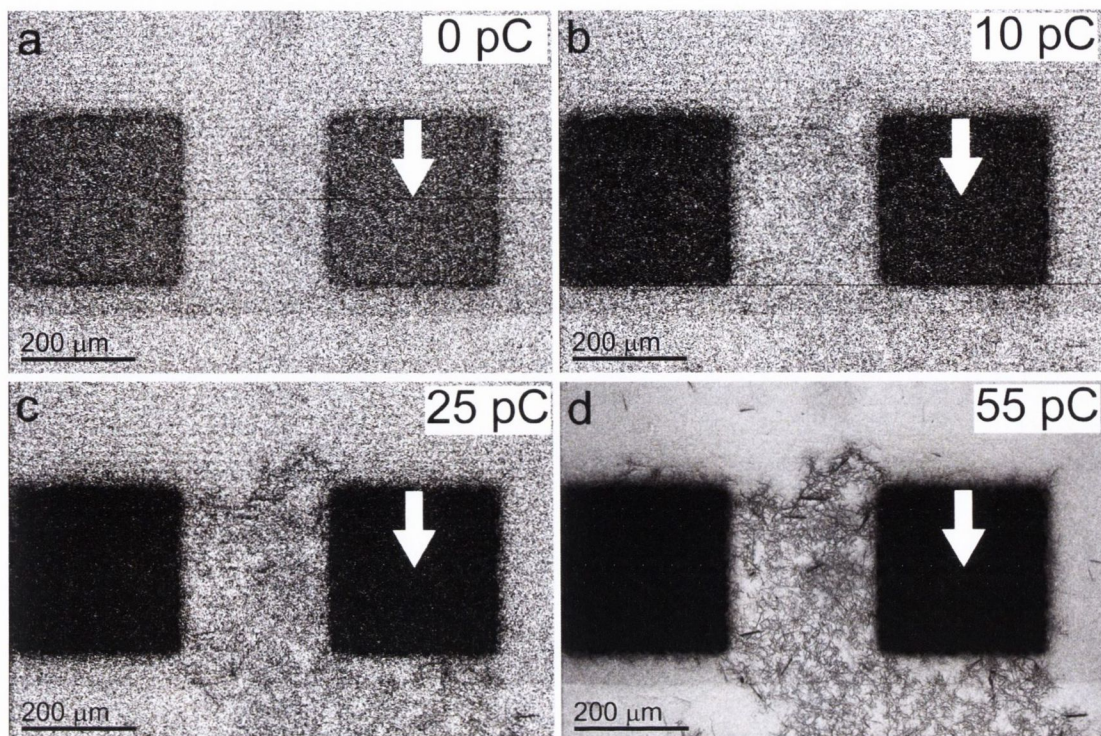
FIGURE 5.16. The effect of dose charge on contrast in HIM PVC images. Dosing a previously activated and evolved network with small, incremental amounts of charge (amounting to a total charge of 55 pC) shows the increasing levels of contrast between activated and non-activated nanowires with charge. The scan time was increased for the image in (d) to improve the quality of the connectivity map.

5.4.1 EFFECT OF CHARGE DOSING

Unlike the SEM PVC technique described in the previous chapter which does not affect the sample, the HIM PVC technique may affect the properties of the network being imaged as the contrast mechanism is dependent upon the magnitude of charge dosed into the electrode. In order to generate a strong enough contrast mechanism, a certain magnitude of charge must be supplied to the sample. Panels a – d in Figure 5.16 show the incremental addition of charge to a previously activated and evolved Ni nanowire network, where the total charge dosed was 55 pC. It is clear that as the dose is increased, the contrast between activated and non-activated wires increases, providing an accurate picture of the network connectivity, and showing that many nanowires that lie outside of the network area have also become activated. Images such as these provide valuable insight into the connectivity of networks.

However, if too much charge is supplied, the potential difference generated may be sufficient to cause charge to hop to nanowires that had not been electrically activated, resulting in a false visualisation of the connectivity – this is termed over-dosing. Figure 5.17 shows the effect of sequentially over-dosing an electrode contacting a $\rho = 0.15\,\mathrm{NW}\,\mu\mathrm{m}^{-2}$ network. The electrode, connected to a previously non-activated network, was dosed with a much larger charge than in Figure 5.16. The arrow indicates the dosing centre in each case,
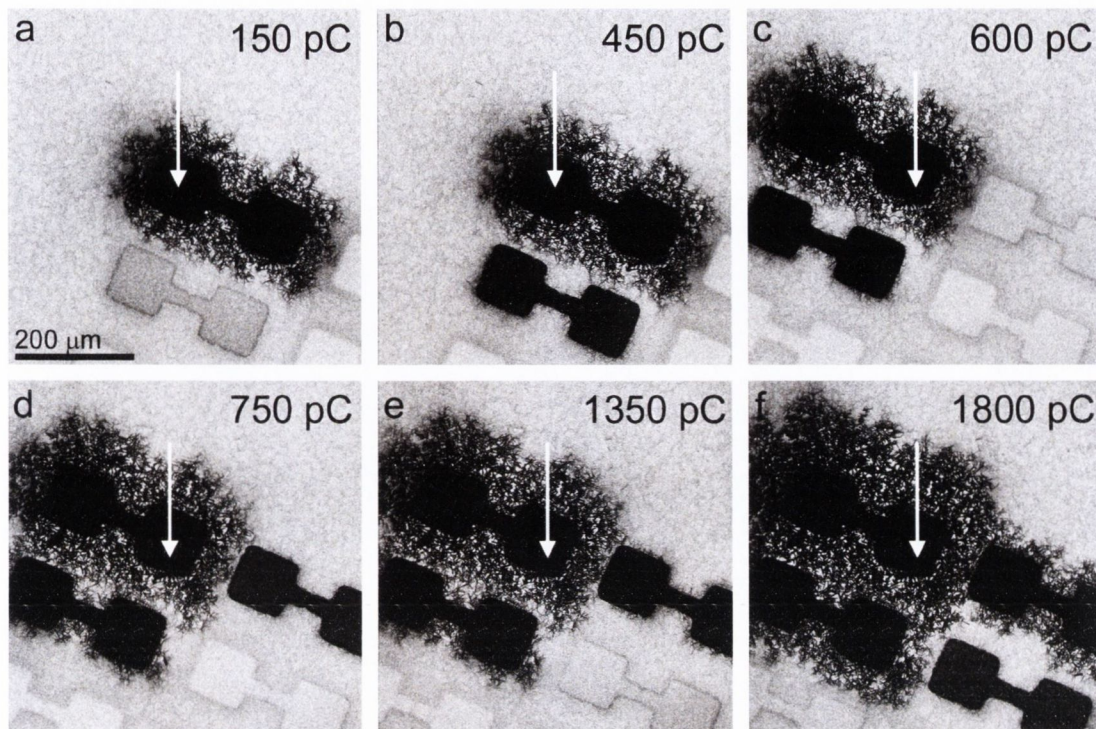
FIGURE 5.17. Sequential dosing of a non-activated network ($\rho = 0.15\,\mathrm{NW\,\mu m^{-2}}$). Images show the expansion of the connectivity cloud for doses of (a) 150 pC, (b) 450 pC, (c) 600 pC, (d) 750 pC, (e) 1350 pC, and (f) 1800 pC. Arrows indicate the dosing centre, that is the point where the beam was focused, in each case.

that is, the point at which the ion beam was focused in order to supply the specified dose. This resulted in a halo or cloud of nanowires surrounding the electrode appearing in the PVC image. As the dose increased to 450 pC, the cloud also increased such that it grew large enough to spread to an adjacent electrode (indicated by the darkening of the neighbouring electrode). The implication of this result is that high dosing levels results in the formation of a conductive pathway between electrodes, however subsequent measurements showed the resistance of the network to be high. It may be that, given the low currents involved, the behaviour observed is a result of junctions undergoing threshold switching, which is unstable at zero bias, and thus the network was subsequently measured in the HRS as the charge had dissipated. To prevent this artificial connectivity evolution from occurring during HIM PVC analysis of networks, it was therefore concluded that the dose should be kept below 50 pC.

The effect of high dose levels on the observed connectivity, while unwanted for visualising pre-activated networks, may provide an alternative method to study the connectivity of these networks. Figure 5.17 (c – f) shows the growth of the connectivity cloud as the dose is increased further, to a maximum of 1800 pC. While these are only initial results, it is clear that there is a relationship between the radius of the connectivity cloud and the supplied dose. Detailed analysis of this phenomenon on an appropriately structured sample
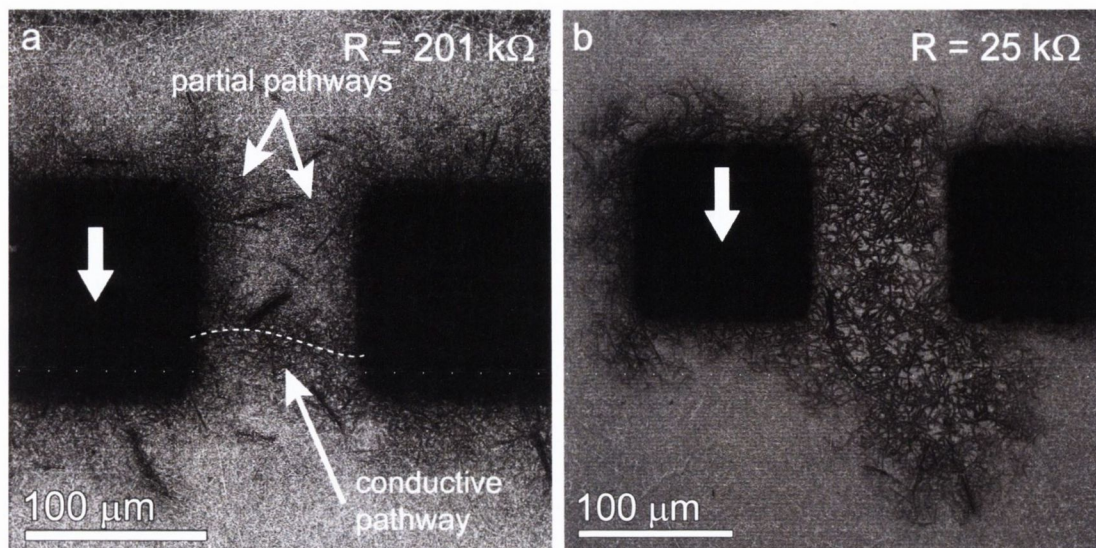
FIGURE 5.18. Comparison of connectivity in two separate networks that have been activated and evolved, respectively, using HIM PVC imaging. (a) PVC image of a network immediately post-activation ($D/L_{NW} = 9.43$; $\rho = 0.64\,\text{NW}\mu\text{m}^{-2}$), where the resistance is still high (201 kΩ). A thin conductive path is visible spanning the electrodes. (b) PVC image of a highly evolved ($R = 25$ kΩ) network ($D/L_{NW} = 9.43$; $\rho = 0.23\,\text{NW}\mu\text{m}^{-2}$). The expansion of the connectivity due to electrical stressing is quite clear, extending beyond the confines of the defined network area.

should thus allow for information regarding the breakdown mechanisms to be elucidated, though this is currently beyond the scope of this work.

5.4.2 CHARACTERISING NETWORK CONNECTIVITY WITH HIM PVC IMAGING

It has been established that by using small (< 50 pC) doses, HIM PVC imaging allows for visualisation of the network connectivity. This may then be used to characterise the connectivity within networks and provide visual evidence for the phenomena described thus far. Figure 5.18 compares the connectivity of two separate $D/L_{NW} = 9.43$ Ni nanowire networks that have been evolved to different resistance states. Shown in Figure 5.18(a), the network was formed to a current level of 10 μA and the resistance measured to be 201 kΩ. Beyond this no electrical stressing was performed, and thus the connectivity of the network should be quite limited. This is confirmed by the PVC image, as a single conductive pathway is observed spanning the electrodes (highlighted in image). Also visible in this image are two incomplete activation pathways (also highlighted). It is likely that when stressed electrically, these pathways will connect and this network will therefore be incapable of exhibiting RS behaviour due to the presence of parallel paths.

In Figure 5.18(b), a fully evolved network is shown. This network was evolved by sweeping a voltage across the electrodes, up to a maximum electric field of 200 kV m^{-1}, resulting in a final network resistance of 25 kΩ. It is immediately obvious from the PVC

image that the connectivity of this network is extensive, reflecting the lower resistance measured. It is also clear that, as in Figure 5.16, connectivity paths extend beyond the area defined by the electrodes, demonstrating the ability of the network to relax the electrical stress by creating many alternative pathways.

The PVC imaging techniques, developed in this work for the study of nanowire networks, provide a unique insight into the behaviour of these fascinating materials, and while each has its own advantages, the results obtained through both techniques described thus far complement each other. It is clear from the images presented in this section that the HIM based PVC imaging technique provides a much stronger contrast between activated and non-activated nanowires compared to those images presented in chapter 4 obtained through SEM PVC imaging. There are a number of reasons for this enhanced contrast. As discussed in chapter 2, the secondary electron yield from HIM bombardment ranges from 3 to 10.[7] There are thus many more electrons contributing to the image of uncharged objects, producing a stronger signal, greater signal-to-noise ratio, and ultimately an enhanced contrast. Additionally, SEM PVC imaging is based on connecting objects to ground, rather than generating a charge to impede the escape of secondary electrons, and is thus a less effective method of modifying electron yield in order to produce contrast. HIM PVC may also provide a unique method of studying network connectivity, as it has been shown that controlled over-dosing of a network produces a connectivity evolution response which may be monitored in real time.

SEM based PVC imaging on the other hand has its own advantages. As only the Inlens detector is sensitive to the enhanced scattering from negatively charged objects, both SE2 and Inlens detectors may be used simultaneously to obtain both detailed topographic and PVC images of the network. By not supplying the sample with excess charge, modification of the network properties through artificial connectivity evolution is not a concern. Additionally, as each electrode must be contacted with a micro-needle attached to ground, in situ electrical measurements are made possible, allowing for the direct study of connectivity evolution with applied bias. Finally, SEM PVC is necessary for the study of low energy barrier materials, such as PVP-coated Ag nanowires, as the charge levels required to produce sufficient levels of contrast in HIM PVC imaging may result in undesired activation/electrical breakdown.

PVC imaging is thus a powerful tool that can not only provide visual confirmation of theories developed thus far in this thesis, but may also be used as an quantitative analytical tool to develop further the ideas of network connectivity. The final section in this chapter draws together the concepts introduced thus far in order to program specific behaviours into a random nanowire network, and demonstrate their simultaneous operation through a simple series circuit.
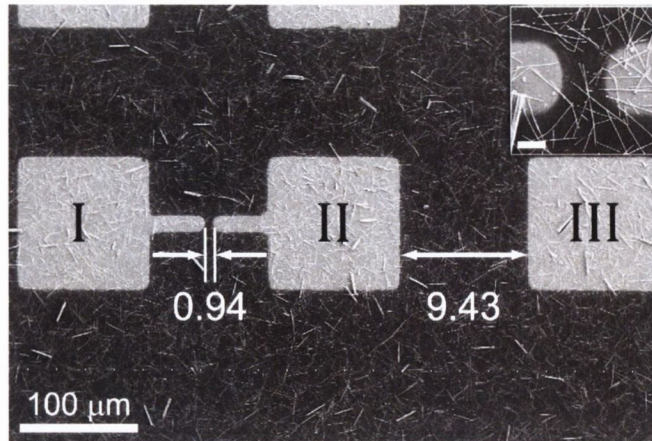
FIGURE 5.19. Programming a nanowire network – part 1. Ni electrodes (labelled I, II, and III) deposited on a $\rho = 0.15\,\mathrm{NW}\,\mu\mathrm{m}^{-2}$ network define two network sizes: $D/L_{NW} = 0.94$ and $D/L_{NW} = 9.43$ respectively. By structuring the electrodes in this fashion it is possible to program different behaviours into the same network. High magnification image of I–II is shown in inset; scale bar is $5\,\mu\mathrm{m}$.

5.5 PROGRAMMING A NANOWIRE NETWORK

Thus far it has been established in this chapter that a Ni nanowire network exhibits different behavioural regimes depending upon the size of the network defined through the electrodes deposited onto it. At small network sizes deterministic RS behaviour is observed, where the resistances of the high and low resistance states are extremely well defined and depend on the length of the conductive path. The reset current however remains constant at all network sizes, implying that a single junction produces the RS behaviour observed. Larger networks, beyond the RS regime, show evolutionary behaviour akin to that exhibited by Ag nanowire networks. The RS character of the junctions shows up in these large networks as an adaptive reconfigurability under large electrical stresses. This ability to control the behaviour demonstrates an intrinsic programmability which stems from the incorporation of resistive switching material at the nanowire junctions, is controlled by the natural geometry of the nanowires, and is thus a fundamental property of networks.

To demonstrate this programmability, a $\rho = 0.15\,\mathrm{NW}\,\mu\mathrm{m}^{-2}$ network was fabricated and two network sizes of $D/L_{NW} = 0.94$ and $D/L_{NW} = 9.43$ were defined by three electrodes labelled I, II, and III respectively, as shown in Figure 5.19. Once formed, the behaviour of the two networks was established by sweeping a voltage across each. The repeatable, deterministic RS behaviour of the network defined by electrodes I–II is shown in Figure 5.20(a). Both V_{SET} and V_{RESET} demonstrate very tight clustering over the three cycles shown, which indicates that the same junctions are switching with each cycle. Under electrical stress, the larger network, defined by electrodes II–III, displayed evolution of the connectivity, achieving a minimum resistance of $29\,\mathrm{k}\Omega$. An I-V curve in the voltage range $\pm25\,\mathrm{V}$ is shown in Figure 5.20(b), showing the linear nature of the I-V response, and demonstrating the stabil-
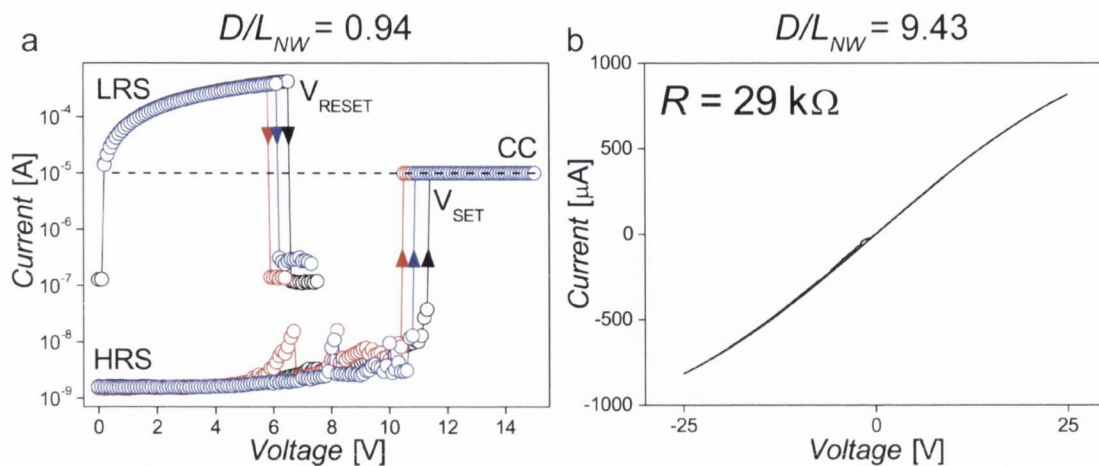
FIGURE 5.20. Programming a nanowire network – part 2. (a) I-V plot measured across electrodes I–II shows repeatable RS, exhibiting the behaviour of a device. The tight clustering of the V_{SET} and V_{RESET} is a strong indicator that the same junction is causing the network to switch in each case. (b) I-V curve taken across electrodes II–III after the network was activated and evolved to its maximum extent, showing a resistance of 29 kΩ. The current is stable in the voltage range ±25 V, exhibiting the behaviour of a material. Sweep rate was 50 mV s^{-1} for all data.

ity of the current in this voltage range. This network thus displays material-like behaviour, in stark contrast to the device-like behaviour exhibited by the adjacent network in close proximity.

To illustrate further the stability of each of these programmed behaviours, a voltage was driven across electrodes I and III. The resulting behaviour was a linear combination of the two programmed regions, demonstrating the device-like characteristics of a RS with the addition of an ohmic load in series. This is shown in Figure 5.21(a), where the RS properties demonstrated by electrodes I–II and I–III are compared. With the RS device in the HRS, a voltage of 11 V applied across electrodes I–III switches the device into the LRS (inset, red circles), approximately equal to the voltage required to set the RS network on its own. As the resistance of the device in the HRS is ~10^2 greater than that of the network, the relative voltage drop across the larger network is negligible, resulting in no contribution to the observed behaviour in this state. The voltage required to reset the device increased considerably however, as the 29 kΩ load now contributed to the total resistance of the system. The value of I_{RESET} was observed not to change, highlighting the dominant role played by the RS device in controlling the behaviour of a large network. Figure 5.21(b) shows the measured current in both HRS and LRS for multiple cycles of the device through electrodes I–III, where the read voltage was 1 V. ON/OFF current ratios greater than 10^5 are demonstrated by the device, even when the LRS resistance is increased due to the added load.

Finally, the programmed network was visualised with PVC imaging. Figure 5.22(a) shows electrodes I, II and II prior to dosing, demonstrating almost no contrast in the image.
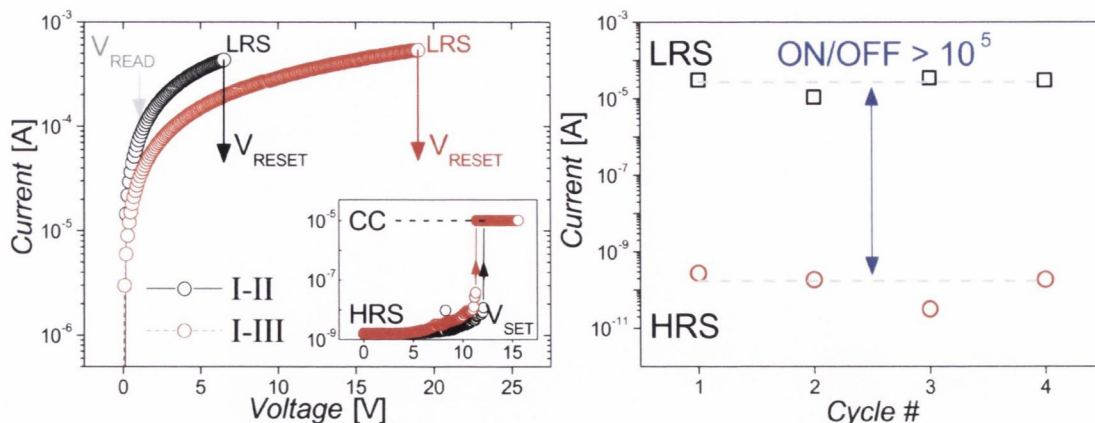
FIGURE 5.21. Programming a nanowire network – part 3. (a) The RS device I–II (black circles) may be operated by addressing electrodes I–III (red circles). The switching properties are modified only slightly, as the resistance of the LRS has increased, thereby pushing V_{RESET} to larger values, while I_{RESET} and V_{SET} remain constant. (b) ON/OFF current ratios greater than 10^5 are observed even while operating across electrodes I-III, where $V_{READ} = 1\,V$. Sweep rate was $50\,mV\,s^{-1}$ for all data.

Electrode II was then dosed with 40 pC of charge generating contrast in all connected objects (Figure 5.22(b)). It is clear that electrodes II and III, as well as the surrounding network, show a strong contrast illustrating that the network has been evolved to a high degree. Electrode I however shows no contrast, reflecting the fact that the RS device was in the HRS. The visible damage to the electrodes is due to scraping of the metal by the sharp probe needles used when making contact. The device was then removed from the HIM chamber, switched to the LRS via a probe station, and then re-imaged (Figure 5.22(c)). Electrode I now displays strong contrast, reflecting the low resistance connection to electrode II. A surprising result is the number of nanowires connected to electrode I that now display contrast, indicating that they had previously been activated. It is possible, by comparing panels (b) and (c), to see that many nanowires lie adjacent to each other between electrodes I and II, yet remain electrically disconnected, as demonstrated by the break in contrast in panel (b). As a result of this, identification of the switching junction was not possible. This result makes the highly controllable nature of the RS phenomenon in networks even more surprising, as it shows that the nanowire connectivity may grow under an electrical stress, yet single junction behaviour will continue to dominate the properties, as long as the network is small enough.
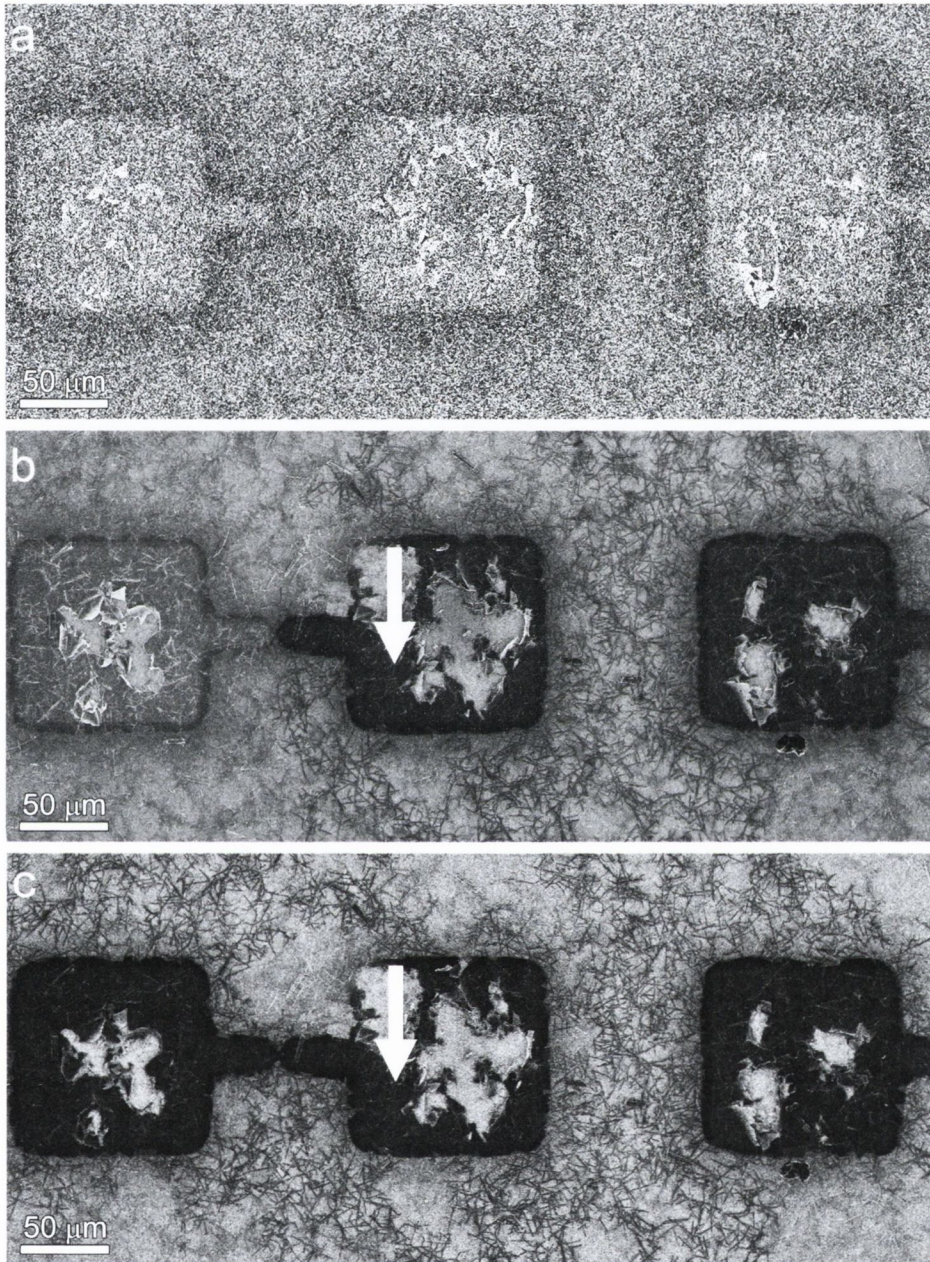
FIGURE 5.22. PVC visualisation of a programmed nanowire network. (a) HIM secondary electron image of the network shown in Figure 5.19, prior to dosing. (b) PVC HIM image of the same network post-dosing 40 pC into electrode II, as indicated by arrow. Contrast is clearly visible in the $D/L_{NW} = 9.43$ network between electrodes II and III. The connectivity extends far outside the defined network area, reflecting the evolved nature of the network. The $D/L_{NW} = 0.94$ network RS device is in the HRS, shown clearly by the lack of contrast in electrode I. (c) The network was re-imaged post setting the RS device to the LRS. Contrast in electrode I and the surrounding network illustrates the LRS of the device. Dosing centre again indicated by arrow.

5.6 DISCUSSION & OUTLOOK

The high voltages required to activate Ni nanowire networks pose a significant challenge to the viability of these materials as oxidation resistant transparent conductors. It was found that the voltage required to activate networks is strongly dependent upon the number of junctions, and that a slope of V_{FORM} vs. D/L_{NW} produces a slope that reflects the value of V_{FORM} for a single nanowire quite closely. Due to the high value of V_{FORM} (3.7 V), it is not possible to activate networks much larger than $D/L_{NW} \geq 50$ as voltages greater than 210 V are required. Additionally, it has been shown in both this and the previous chapter that electrical stressing alone is not sufficient to maximally evolve the connectivity of a large network. To overcome these limitations, methods are currently being developed to achieve network wide junction activation, however for now Ni nanowire networks are not a viable material for use as oxidation resistant transparent conductors despite their excellent resistance to atmospheric degradation.

The HIM PVC technique developed in this work to visualise the connectivity is an extremely powerful one, and has many potential applications outside the study of networks. The contrast generated through dosing a sample with charge is much greater than that obtainable through an equivalent SEM technique due to the greater number of secondary electrons produced. While the technique may not be viable for certain sensitive device applications due to the potential risk of dielectric breakdown caused by excessive charging, it has been demonstrated here that it is possible to carefully limit the charge dose such that this is avoided. This technique is therefore expected to be extremely valuable for the mapping of electrical connectivity in complex systems. The result of PVC imaging in both this chapter and those presented in chapter 4 demonstrate that driving connectivity evolution results in the formation of conductive pathways far outside the active device area defined by the electrodes. This highlights the need to develop methods to define isolated networks in order to study more quantitatively these materials, but also for any future device applications. To this end, methods are currently being developed using a combination of EBL in conjunction with existing spraying techniques to fabricate isolated networks of arbitrary shape and size.

The central result of this chapter is the discovery that a random network of nanowires may be programmed to exhibit multiple behavioural states, based on the scale of the network addressed. It has been clearly shown that small networks demonstrate the RS properties of single Ni/NiO/Ni junctions, and that as the network is made larger these junction properties cease to dominate the network behaviour, ultimately producing two behavioural regimes displaying device-like, and material-like properties respectively. Programmability is thus a direct result of the incorporation of a unipolar RS element at the nanowire junctions. The results presented here are in contrast with those published by Gimzewski and Stieg et al. at UCLA. Discussed in chapter 1, they show that a network of bipolar resistive switching junctions, when addressed electrically, exhibits a global response consisting of contributions from the entire network,[8] rather than the discrete activation pathways observed in this work. Additionally, they show a large network (exact size not defined) exhibiting a bipolar

RS response, rather than the evolutionary material-like behaviour observed in this work for large network sizes.[9] These comparisons highlight the need to identify behaviour in individual systems so that the overarching laws governing the properties of random networks may be elucidated. These results demonstrate that small variations in the properties of the junctions can result in vastly different properties of the network.

Network programmability is thus a novel discovery, and the results presented here are transferable to other network systems, thus providing a blueprint for the design of programmable materials from random percolative networks. Programmability will enable application in technologies where ease of fabrication, low cost, and maximum transparency/flexibility are a high priority such as artificial skin and sensing applications. Indeed, the demonstrated ability to act as both device and interconnect suggests very low cost sensor technologies.

5.7 CONCLUSIONS

The work presented in this chapter focused on studying the electrical behaviour of Ni nanowire networks as a function of network sizes. It was found that V_{FORM} scales linearly with network size, also showing a dependence on network density, consistent with the results obtained in chapter 4. The behaviour of small ($D/L_{NW} \leq 10$) networks was found to be dominated by the resistive switching properties of the individual junctions, and it was concluded that single junctions are responsible for the behaviour observed even at the larger network sizes. For larger networks ($10 \leq D/L_{NW} \leq 50$), it was found that the connectivity evolution behaviour observed for PVP-coated Ag nanowires dominates the properties of the Ni nanowire network. By combining electrical characterisation with a novel helium ion microscope based passive voltage contrast imaging technique, the evolutionary behaviour of these networks was characterised. Additionally it was demonstrated that dosing a network with charge in a HIM caused the connectivity to grow, allowing for step-wise characterisation of the connectivity evolution, and this is a potential area of further study.

Ultimately, it has been shown that these networks exhibit properties that not only evolve and adapt in response to electrical stimuli, leading to controlled levels of connectivity and conductivity, but that the incorporation of RS elements introduces levels of programmability not available in conventional materials. Networks are intrinsically programmable due to their capacity to dynamically reconfigure the distribution of ON and OFF junctions leading to fault-tolerant and adaptive behaviours. The natural length scales defined by the nanowire dimensions, the size of the connectivity cells and the separations between electrodes define a physical programmability whereby the properties of the confined network can be controlled and exploited for material and device applications.

REFERENCES

[1] BELLEW, A. T., BELL, A. P., MCCARTHY, E. K. ET AL., *Nanoscale* **2014**, *6*, 9632–9639.

[2] SOREL, S., LYONS, P. E., DE, S. ET AL., *Nanotechnology* **2012**, *23*, 185201.

[3] RUSSO, U., IELMINI, D., CAGLI, C. ET AL., *Electron Devices, IEEE Transactions on* **2009**, *56*, 193–200.

[4] PRALL, K., RAMASWAMY, N., KINNEY, W. ET AL., in *Memory Workshop (IMW), 2012 4th IEEE International*, IEEE, pages 1–5.

[5] ITRS, The international technology roadmap for semiconductors, Technical report, http://www.itrs.net/, **2013**.

[6] DUMAS, C., DELERUYELLE, D., DEMOLLIENS, A. ET AL., *Thin Solid Films* **2011**, *519*, 3798 – 3803.

[7] WARD, B. W., NOTTE, J. A., and ECONOMOU, N. P., *Journal of Vacuum Science and Technology B* **2006**, *24*, 2871–2874.

[8] STIEG, A. Z., AVIZIENIS, A. V., SILLIN, H. O. ET AL., *Advanced Materials* **2012**, *24*, 286–293.

[9] STIEG, A. Z., AVIZIENIS, A. V., SILLIN, H. O. ET AL., *Japanese Journal of Applied Physics* **2014**, *53*, 01AA02.

6

CONCLUSIONS

This thesis has explored the field of nanowire networks, and attempted to answer certain questions regarding the connectivity of nanowires within networks, and how this may be affected through manipulation of the nanowire junction. Networks are a material of growing technological interest due to their inherent properties of high transparency, flexibility, ease of fabrication, and in certain cases extremely low resistance. Notable technologies where nanowire networks have been incorporated, in a lab setting at least, include transparent conducting screens, solar cells, electronic/artificial skin, and various sensing technologies. To date, the study of these materials has largely focused on optimising these bulk properties by manipulating nanowire geometry, fabrication conditions, or post-fabrication treatments and processing. This represents a top-down approach to optimisation; and while this approach has produced some remarkably high performing materials, shortcomings remain. In particular, combining experiment and simulation to achieve a more fundamental understanding of the network properties has thus far produced inconsistent results. At the heart of the matter is the understanding of the nanowire-nanowire junction. The fundamental unit of a network, junctions play a pivotal role in determining the ultimate performance of the film. This thesis took a bottom-up approach to studying networks by focusing on individual junctions, and beyond this looked at networks of increasingly larger size to develop a thorough understanding of the impact that junction properties have on the behaviour of the network as a whole.

Ag nanowire networks are currently the highest performing transparent conducting material compared to indium tin oxide, the current industry standard. The junction resistance of Ag nanowires reported in the literature is still a matter of debate, with no studies to date reporting measurements on multiple junctions. Typically fabricated through the well-known polyol process, Ag nanowires are formed with a thin (1–2 nm) coating of polyvinylpyrrolidone (PVP), an insulating polymer that in normal use must be removed through a post-fabrication treatment in order to create a high performance conductive network. For this work however it provided the perfect system to study the resistance properties of single

junctions by comparing the junction resistance of nanowires that had been thermally treated to remove the PVP, and those that hadn't. In order to accurately measure the resistance of individual junctions, a combination of UV lithography and electron beam lithography was employed to fabricate thin metal contacts onto the nanowires that formed a junction in a 4-probe geometry. This allowed resistance measurements to be made that took account of the contact resistance. The resistance contribution from the nanowires was accounted for by confirming the resistivity to be that of bulk Ag, and performing accurate measurements of the nanowire geometry using AFM and SEM, thereby allowing an accurate value for the resistance of the junction to be extracted.

Junction resistance measurements were performed on multiple nanowires that had been both thermally annealed to remove the PVP layer, and those that had undergone no processing prior to being contacted. The results of the thermally annealed wires showed very low junction resistances below 50 Ω. It was found that non-annealed junctions demonstrated an irreversible switching of the resistance from the pristine, non-conducting state to a highly conductive state upon application of a sufficiently large voltage across the junction. It was found that the resistance of this electroformed junction could be optimised by driving current through it, and it was proposed that the mechanism behind this current-induced junction enhancement was the Joule heating resulting from the high current densities experienced at the nanoscale interface, effectively performing a localised anneal. Although on average not as low as the thermally annealed junctions, the electroformed junctions still produced low resistances, typically displaying values below 60 Ω. The results of both thermally and electrically activated junctions were combined to produce the first distribution of measured junction resistances consisting of 16 junctions, demonstrating a mean value of 58 Ω and a median value of only 23 Ω. An SEM study of the measured junctions showed that the thermal annealing step tends to create welded junctions, and while these demonstrated low resistances, welding was not necessary to obtain highly conductive junctions.

This result has significant implications for research on Ag nanowire networks. Prior studies have consistently overestimated the resistance contribution of the junction. This is primarily due to a failure to perform 4-probe measurements and therefore not taking the contact resistance into account, in addition to only reporting results of a single junction. The results obtained in this work align well with those presented in a study by Lee et al. in 2008, which estimate the junction resistance from bulk sheet resistance measurements and find it to lie in the range 1–100 Ω, consistent with these findings. These results have another important implication for the field of transparent conductor research. The spread in junction resistance values obtained in this study suggests that a large proportion of the junctions within a so-called optimised network are still relatively highly resistive, and therefore imply that the lowest sheet resistances are not yet being obtained. This suggests that there is further room to improve the resistance of these networks, and thus the development of new methods to optimise network resistance must be a key area of focus in the coming years. This work therefore represents a significant contribution to the field of nanowire network research.

Ni nanowires represent a material system that is structurally quite similar to, but behaviourally very different from PVP-coated Ag nanowires. Having a thin layer of naturally forming insulating oxide, Ni nanowires are core-shell structures and thus an as-formed junction is non-conducting in the pristine state, as for Ag. NiO is a material well known to display resistive switching (RS) properties when sandwiched between two metal electrodes, and thus a Ni nanowire junction, consisting of two Ni cores separated by a layer of NiO, forms a natural RS structure. The resistance of such a junction then depends on the properties of the metallic filament spanning the oxide, thereby providing a means to indirectly analyse the properties of the filament. Measurement of the junction resistance for Ni nanowires is significantly more complicated than the Ag equivalent, as each metal-nanowire contact must be switched to a conducting state. Additionally, the oxide thickness of the nanowires, measured by TEM analysis, must be taken into account while computing the resistance of the nanowire length, introducing greater uncertainty to the final measurements. The junction resistance of Ni nanowires was found to be much higher than that of Ag, as expected, averaging $718\,\Omega$ with a standard deviation of $437\,\Omega$. It was also shown that after cycling the resistive switching junction multiple times, the junction resistance varied by as much as $100\,\%$, demonstrating that the properties of the filament are continually fluctuating between cycles despite no change in external conditions. These are the first measurements of their kind, and thus represent a novel contribution not only to the field of nanowire networks, but to that of resistive switching.

Core-shell, metal-insulator systems such as PVP-coated Ag nanowires provide an excellent model from which to begin studying connectivity in random networks. It was established that non-annealed Ag nanowires provide a barrier to conduction in the initial state, but that through the action of an electric field this may be broken down to produce a highly conductive connection. The same must also be true of a network of these materials. By studying the activation and subsequent electrical stressing of these networks, information was gained regarding the interplay between the properties of the junction and those of the network as a whole. A conductive-AFM study mapped the activation of nanowires at various distances from a contacting electrode, showing that the activation voltage is dependent upon both the inter-electrode distance and the nanowire density. Using the results of this study as a basis, a model was developed to describe the activation of networks. It was concluded that small cells of activated nanowires form through a local cascade mechanism, and that the size of these cells is a function of both the applied voltage and the distribution of junction breakdown voltages, $\rho(v_B)$, present in the system. Ultimately a conductive path is formed between interrogating electrodes when these activation cells grow to such a size that they overlap.

Building upon this earlier work on network activation, the post-activation electrical behaviour of Ag nanowire networks was examined as a function of network size. The electrical behaviour of networks, fabricated using spray deposition, was examined by contacting electrodes formed by metal evaporation through a shadow mask, where the inter-electrode distance defined the network size. By monitoring the current-voltage response of the net-

work under electrical stress, it was found that networks of all sizes display hysteresis in the current response, described as connectivity evolution. To help explain this behaviour, a novel SEM-based passive voltage contrast imaging technique was developed that enabled the visualisation of conductive pathways through a network. Combining the results of electrical measurements with PVC images, it was concluded that connectivity evolution occurs due to contributions from two phenomena: current-induced junction resistance enhancement, and activation of alternate conductive pathways. By comparing maximally stressed networks with thermally annealed networks of equal density, it was shown that the resistance to which a network may be evolved (taken as a proxy for degree of connectivity) is dependent upon network size. A $D/L_{NW} = 5.48$ network was driven to achieve a minimum resistance of $63 \, \Omega/\square$, approximately equal to the annealed network resistance of $77 \, \Omega/\square$, while a $D/L_{NW} = 137$ network reached a minimum resistance of $315 \, \Omega/\square$, indicating that there remain many more nanowires yet to be activated. It was thus shown that the connectivity, and thus the conductivity, of PVP-coated Ag nanowire networks may be manipulated through the action of an electric field. This demonstrates a novel material with a tunable resistance, where the precision to which the resistance may be tuned is a function of both network size and density.

Passivation layers are ubiquitous throughout the field of nanoscience. In order to prevent aggregation of nanostructures, a surface layer (such as PVP, but other examples include citrate or thiol molecules) must be used to functionalise the surface. While beneficial for fabricating and stabilising nanostructures, these passivation layers must then be removed before a functional device or technology can be realised, and thus present a major barrier to the implementation of nano-materials in new technologies. The work on PVP-coated Ag nanowires presented in this thesis demonstrates that passivation layers are not necessarily always an obstacle, but in fact may be utilised to produce new materials with novel behaviours. The electrical breakdown of PVP is an irreversible process however, resulting in unidirectional network behaviour. As a reversible, resistive switching passivation layer, NiO presents an alternative to PVP to study the effect of a reversible junction on the behaviour of a larger network. It was shown that, while still governed by the same laws as that of the Ag-PVP system, the incorporation of a RS element at the junction introduces the ability to program a network for different behaviours.

To investigate the effect of reversible junctions on network properties, the electrical behaviour of Ni nanowire networks was studied as a function of network size. It was found that small networks ($D/L_{NW} < 10$) exhibit the same resistive switching behaviour as in single junctions, and demonstrate a scaling of the parameters V_{SET} and V_{RESET} with increasing network size. However I_{RESET} was shown to be independent of network size as all network sizes were observed to have reset current values equivalent to those observed for single junctions. It was therefore concluded that single junctions are responsible for the switching behaviour observed, even at the larger network sizes. By establishing the switching probability, P_{RS}, it was found that the tendency to demonstrate RS drops off significantly beyond a network size of $D/L_{NW} \approx 5$. Rather than resistive switching, larger networks

$(D/L_{NW} > 10)$ display hysteretic current-voltage behaviour, mirroring the behaviour of Ag networks, and indicating the evolution of connectivity.

A novel passive voltage contrast technique, based on the helium ion microscope, was developed to image the connectivity in Ni nanowire networks. This PVC technique demonstrated substantially greater contrast between activated and non-activated nanowires than that shown for SEM-based PVC, allowing the network paths to be easily mapped, and the connectivity evolution concepts to be clearly visualised. Additionally, it was found that the connectivity of a non-activated network could be artificially developed by dosing it with large amounts of charge via the He ion gun – a process termed over-dosing. Although only early results were presented, this method provides a unique way to qualitatively map the connectivity evolution in these materials. These results demonstrate that the incorporation of a resistive switching element at the nanowire junction results in the emergence of distinct behavioural regimes that are a function of the network size; this ultimately demonstrates an inherent programmability of the network behaviour that originates from the properties of the junctions, and which is controlled by the geometry of both nanowire and network. These concepts were ultimately brought together to show that the same network could be programmed to act as both a RS device and a metallic interconnect material.

The results presented in this thesis pose more interesting questions to be answered in future work. For example, the effect of incorporating both inter-wire and junction resistances into calculations of the total network resistance must be understood. As discussed in chapter 3, previous attempts to model these systems have produced inconsistent results. To this end, the fruitful collaboration with Prof. Mauro Ferreira will continue in order to combine the bottom-up experimental results obtained in this work with a rigorous computational model, and create a powerful new approach to network design. This new approach will enable the complete range of properties exhibited by a random network of metallic nanowires to be computed, as long as fundamental parameters such as the junction resistance are known. This melding of experiment and computational power holds enormous potential to completely transform the way these materials are studied.

One topic not discussed at any real length in this work is threshold switching, i.e. the deactivation of a conductive pathway (or filament) upon removal of an external bias. This behaviour, along with resistive switching, appears to be somewhat ubiquitous in nature. By limiting the current passing through a thin filament, for example in a single nanowire junction, the size and strength of that filament are also limited. At room temperature, the diffusion of the constituent atoms may proceed to dissolve the filament, breaking the electrical connection and returning the device to a high resistance state. This phenomenon is of great technological importance, as the linear combination of memory and threshold switching elements may enable extremely high density, non-volatile memory arrays. Further study of this phenomenon in the context of single nanowire junctions is proposed for both Ag and Ni nanowires. Both the current dependence and temporal dependence of the threshold switching phenomenon shall be explored, with the aim of developing an empirical model for this process. This work will enable further optimization of the network resistance for

transparent conducting applications.

Finally, whilst the impedance spectroscopy analysis of single junctions presented in chapter 3 was not successful in measuring the capacitance contribution of a single junction, it remains a question of considerable importance, and as such work in this area shall continue. In collaboration with Dr Paul Hurley in Tyndall National Institute, the substrate and device geometry will be completely revised, reducing the parasitic capacitance as much as possible and therefore enabling these extremely sensitive measurements to take place. Additionally, the possibility of monitoring the pre-activation breakdown behaviour of a network shall be explored by monitoring the transient currents generated as individual junctions become shorted. This will add to the growing knowledge base of these material systems and help further develop the physics governing their behaviour.

The nanowire junction is the fundamental building block of a nanowire network, and its properties are the determining factor behind the performance of that network. This thesis has shown that it is not only vital to perform direct, fundamental measurements of individual junctions, but that incorporation of novel materials that modify the junction behaviour allow us to study otherwise hidden properties such as network connectivity, which in turn lead to new material behaviours such as connectivity evolution. By developing our understanding of the nanowire junction and its role in determining network behaviour, it is then possible to begin to modify the junction to add new, novel functionality into these materials which ultimately leads to the ability to program a random network.

A

SCALING OF V_T AT INTERMEDIATE INTERELECTRODE SPACINGS

The following proof was provided in the supplementary information in Nirmalraj, 2012.

In order to evaluate the integral in equation (4.4), the functional form of both the local voltage drop, v, and the distribution, $\rho(v_B)$, must be known. It is suggested that v depends on the interelectrode spacing, D and the average inter-junction separation $\langle \delta \rangle$, according to:

$$v = \frac{V}{D/\langle \delta \rangle} = \frac{V}{D}\sqrt{\frac{A}{N}} \tag{A.1}$$

It is also assumed that $\rho(v_B) = b\,v_B^{\beta}$, where the sign of β determines the rising and trailing sides of the function respectively. Evaluating equation (4.4) then produces:

$$V_T = \left(\frac{a^2 b}{\beta+1}\right)^{\frac{1}{2-\beta}} \alpha^{\frac{\beta-1}{2(\beta+2)}} D^{\frac{\beta+1}{\beta+2}} \left(\frac{N}{A}\right)^{\frac{\beta-1}{2(\beta+2)}} \tag{A.2}$$

It was shown experimentally (Figure 4.3(b)) that at large D, $V_T \propto (N/A)^{-1/2}$. Therefore $\beta = -\frac{1}{2}$, and $V_T \propto D^{-1/3}$.