A Single Nanoscale Junction with Programmable Multilevel Memory

Curtis O'Kelly, Jessamyn A. Fairfield, and John J. Boland*

School of Chemistry, Trinity College Dublin, Dublin 2, Ireland
CRANN Institute, Trinity College Dublin, Dublin 2, Ireland
Single Nanowire, TiO2, Memristor, Multilevel Memory

ABSTRACT: Nanoscale devices that are sensitive to measurement history enable memory applications, and memristors are currently under intense investigation for robustness and functionality. Here we describe the fabrication and performance of a memristor-like device that is comprised of a single TiO_2 nanowire in contact with Au electrodes, demonstrating both high sensitivity to electrical stimuli and high levels of control. Through an electroforming process, a population of charged dopants is created at the interface between the wire and electrode that can be manipulated to demonstrate a range of device and memristor characteristics. In contrast to conventional two-terminal memristors, our device is essentially a diode that exhibits memristance in the forward bias direction. The device is easily reset to the off state by a single voltage pulse and can be incremented to provide a range of controllable conductance states in the forward direction. Electrochemical modification of the Schottky barrier at the electrodes is proposed as an underlying mechanism, and six-level memory operations are demonstrated on a single nanowire.

Transition metal oxides are an emerging candidate material for the realization of non-volatile, low power memory devices for handheld and portable electronics.[1, 2] Non-volatile memories that retain encoded information without power consumption would greatly enhance battery performance for all mobile platform technologies.[3] Recent devices based on transition metal oxides display many characteristics required for the next generation of resistive switching based random access memory (RRAM) technologies.[4-9] TiO_2

has been the focus of much research since it was predicted to enable a specific type of RRAM operation known as memristance.[10] In principle, a memristive device can operate along a continuum of resistance states between the traditional high resistance state (HRS) and low resistance state (LHS) found in conventional resistive switching devices, with the evolution of the resistance state controlled by the flow of charge through the device.[11] In practice, the level of performance has yet to match that described in the memristor simulations.[12, 13] However, if reliability can be improved, memristors have the potential to enable novel multilevel or multibit coding paradigms, storing more information per unit memory cell and maintaining this information without consuming power. Although a variety of multilevel memory devices have been proposed,[14, 15] it has proven difficult to program the number of levels with high fidelity and a large on/off ratio.

To date, resistive switching and memristance have been demonstrated in planar thin film devices in which the controlled resistance is achieved by the action of charged mobile dopants within the active device layer.[16-19] The conventional memristor is a two-terminal device in which a nanoscale film of active material (TiO_2 in this case) is sandwiched between metal electrodes. In this report, we use a TiO_2 nanowire as the active device material and demonstrate that a *single* electrical contact to this wire can be engineered to create a memristor with unique performance characteristics. We show that in addition to the controlled evolution of the current levels and hence the conductance of the device, it is possible to reset the device by the application of a single voltage pulse, and to precisely increment the conductance states of the device to implement multilevel memory that is more robust and reliable than has previously been shown in TiO_2. We show that our device effectively operates as a unipolar memristor diode, and discuss plausible mechanisms of device operation and advantages over conventional planar two terminal structures.

RESULTS AND DISCUSSION

Each device consisted of a single crystal TiO_2 nanowire and two Au contacts, as shown in Figure 1(a). Whereas the device is initially symmetric, in all subsequent processing steps one of the electrodes is held at ground and used as a reference throughout. In its virgin state the device is a poor conductor. To probe

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the initial state of the virgin device, a +10 V sweep is applied at a rate of 0.23 V/s (total time ~130 s) while the current levels are monitored. Current typically ranges from 10–1000 pA for individual devices. The black curve in Figure 1(b) shows a typical current trace for a virgin device. The current rises above the noise threshold level at around +7 V during the initial voltage sweep, and there is clear hysteresis in the current trace as the bias is swept to +10V and then back to 0V. The direction of the hysteresis loop is indicated by the arrows in Figure 1(b).

The current levels within the nanowire device can be significantly increased by undergoing an electro-forming step similar to those used for planar thin film TiO_2 devices.[16, 17, 20] This involves the application of a steady state voltage (typically +10V) for a sustained time period (typically 1000 s) while the current is monitored with a set compliance limit of 1 nA. The red curve in Figure 1(b) shows the difference in current levels for the same device before and after the forming step. The maximum current is increased and the turn-on voltage is reduced to +1.5V, comparable to the turn-off voltage for the device in its virgin state. This electroforming step changes the properties of the wire in the vicinity of the positively biased electrode (see below) and increases the overall conductance of the device. Similar behavior is observed for a device under negative bias conditions, except that the modification of the wire occurs at the electrode that is grounded (see Supporting Information Figure S2).

Current levels within the device can be developed further by successive electroforming steps at higher set compliance values or through continuous and repeated application of voltage sweeps. Continuous voltage sweeps reveal the dynamic behavior of the nanowire device and also provide insight into the physical mechanism of operation. Figure 2(a) shows the evolving current response to a series of 8 voltage sweeps. The conductance of the device increases incrementally with each applied sweep, up to a maximum conductance value. By the 8th sweep, the current levels no longer increases with additional voltage sweeps, and the device response collapses into a stable repeating hysteresis loop. The turn-on and off voltages also collapse onto a single value, +1.5 V in this case. Under this condition, the device remains in a stable or 'saturation state' (SS). All devices display this dynamic behavior in response to repeated

voltage sweeps. The SS condition provides a useful reference state for the device and to which the device can always be returned. This is important for a dynamic memristor-like device which, by its nature, is susceptible to changing state in response to the voltage, current, and sweep rate conditions it is exposed to. The SS represents a stable reproducible state in an otherwise dynamic and continuously evolving device operation space.

Changing the frequency of the applied voltage sweep also greatly affects the electrical properties of the device, as seen in Figure 2(b). In each instance the device was brought to the SS associated with that frequency. The different traces in the figure have been offset for clarity. The maximum sweep rate is 5 Hz, which is slow but reflects the > 2 μm size of the device. Altering the frequency of the applied voltage sweep affects two aspects of the device current-voltage response. Firstly the maximum current becomes diminished for faster voltage sweeps while secondly, the breath of the hysteresis loops become notably collapsed at higher frequencies. Both behaviors are characteristic properties of memristors as described by Chua and Williams *et al*, despite the fact that our device does not have the conventional two-electrode sandwich memristor geometry.[10, 11]

Figure 2(c) shows the phase angle between the drive voltage and current recorded during the measurement of the SS in Figure 2(a). A phase angle of -90 degrees is consistent with a capacitive response that dominates the initial low voltage behavior of the device, however at larger voltages the response is resistive indicating the establishment of improved electrical conduction between wire and the metal contact. This behavior is consistent with the presence of a blocking capacitor at the device interface that becomes increasingly transparent at high applied voltages.

Figure 3(a) shows the response of a device specifically prepared to be in the SS to a bipolar voltage sweep. As expected, the device initially displays the SS response during first positive voltage sweep (red curve labeled 1 in figure), similar to the response seen in Figure 2(a). On the other hand, no significant level of current is observed during the negative voltage sweep (2), indicative of diode-like behavior. The second positive voltage sweep (3) reveals a current response albeit at a lower level than that observed in

the first sweep. Our device is therefore essentially a unipolar memristor, and thus the application of a negative voltage pulse can be used to systematically step back or reduce the conductance at positive biases. Note however that the application of a sustained negative voltage eventually quenches the device conductance in the positive voltage direction, resulting in the growth of the same device characteristic seen in Figure 2, except at negative voltages with the electroforming phenomenon at the grounded electrode (see Figure S2).

This ability to reset or step back the conductance in the forward channel by applying a reverse bias pulse is not available in conventional memristors and enables improved control of device operation and enhanced performance. Thus we can apply a -7.5V pulse to reset the device, following which we examine the device response to a subsequent series of positive set pulses. Figure 3(b) shows the combined effect of a -7.5 V reset followed by five +7.5 V set pulses for a device that was originally in its SS defined by a 18 nA saturation current at +7.5 V. The pulse width is 2.5 sec in duration. Each positive voltage pulse increments the device conductance by a specific amount while the device can be quantitatively reset using a negative pulse. The resulting six-level memory device in Fig 3(b) has high current fidelity and precisely controlled levels compared to previous multilevel memory devices.[21, 22] The observed on-off ratio is excellent, as expected for high-purity TiO_2.[15] Figure 3(c) shows the time evolution of the six-level memory device from the beginning of the pulsing sequence. We note that the device response evolves during the initial cycles but beyond 60 pulse applications it saturates into six well defined conductance levels, from which the data in Fig. 3(b) was recorded. This initial behavior is consistent with that seen earlier in Figure 2(a) and typical of memristor devices in general,[10] which exhibit a temporal response to any voltage stimulus. Critically, the relative separation between the memory levels remains unchanged even during the initial period. This is underscored in Fig 3(d) which shows the magnitude of the current at each level as a fraction of the highest current level. Despite the initial induction period the relative magnitudes are essentially constant throughout. Once steady state has been achieved the conductance values associated with each memory level are defined to better than 3%. By changing the pulse combination or by tuning the pulse height and width before the reset pulse, it is possible to change the number of memory levels

that span the maximum current level the device can support. Supporting Figure S3 shows the case of a four-level memory device. The status of the multilevel memory levels is read by the application of a sub-threshold voltage pulse large enough to produce a measurable current, but not capable of modifying the conductance. Threshold behavior is a characteristic memristor property and in our case the optimum read pulses are between +3 V and +5 V.[12]

The mechanism of resistive switching and memristance in TiO$_2$-based device is widely debated in the literature.[23] Here we hypothesise on the operation of our device in the context of what has been reported. We begin by considering the band alignment across the device structure shown in Figure 1(a). The Au contact leads have a work function of 5.1 eV and form Schottky barrier contacts with the wide bandgap TiO$_2$ nanowire. Since the nanowire is single crystal with a high degree of perfection, few carriers are available to screen the Schottky barrier, so that the presence of the latter likely dominates the measured conductance of the virgin wire. This situation is described schematically in Figure 4(a) where band bend-ing reflects the Schottky barrier height and width. Under electroforming conditions described here oxy-gen vacancies are known to readily form at the TiO$_2$ interface with the positively biased Au metal con-tact.[16, 17, 20, 24, 25] These anodic conditions result in the oxidation of the lattice oxygen $O_O^\times$ to form positively charged oxygen vacancies $V_O^{\bullet\bullet}$ by the following reaction:[26]

$$O_O^\times \rightleftarrows V_O^{\bullet\bullet} + 2e' + \tfrac{1}{2}O_{2\,(g)} \qquad\qquad (1)$$
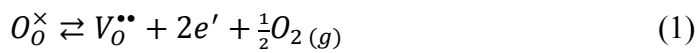
It is well established that oxygen vacancies act as n-type dopants with shallow donor states below the conduction band of bulk TiO$_2$.[27] This has the effect of shifting the Fermi energy closer to the bottom of the TiO$_2$ conduction band, as shown in Figure 4(b), thereby increasing the number of free electrons in the band. The oxygen vacancies generated by reaction (1) may form a charged double-layer with the negative sheet of charge on the Au electrode established during Schottky barrier formation.[26] This double layer is a capacitor and may be the origin of the capacitive behavior seen in the impedance data in Figure 2(c).

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The additional carriers created by this reaction will reduce the Schottky barrier height and width and increase the rate of tunneling into the contact. If a sufficiently large population of vacancy dopants are created and extend beyond the interface, an impurity band could form that facilitates conduction by a variable range hopping mechanism.[28]

An important aspect of the device operation is that positively-charged oxygen vacancies that are created at the anode are mobile. While mobility is necessary to establish the charge double layer described above, any penetration of an applied electric field through the double layer will naturally cause the oxygen vacancies to drift away towards the cathode. Based on this we suggest that the SS condition described in Figure 2(a) reflects a balance between the rate of vacancy generation at the anode and the rate of vacancy drift towards the cathode. Crucially, the application of a short negative (reset) voltage pulse has the effect of injecting electrons from the Au electrode into the wire, annihilating oxygen vacancies in the near contact region *via* the reverse of reaction (1). This creates a depletion region next to the Au electrode and effectively resets the device, consistent with the data in Figure 3. Subsequent set pulses sequentially restore the oxygen vacancy population. This unique reset ability provides an important handle in controlling the multilevel memory operation.

The device reported here has parallels with conventional planar $Au/TiO_2/Au$ memristors, except that by comparison the thickness of the TiO_2 layer in this device is very large, which effectively separates the behavior of the device at the two electrode regions so that they can be treated independently. In contrast, a conventional planar memristor typically has an oxide layer that ranges in thickness from 20-50 nm, and both electrodes are involved in the creation and/or subsequent reaction of mobile charge dopants responsible for device operation. Issues such as dopant discharge at the counter electrode are common.[12] An obvious attraction of the device geometry in Figure 1(a) is the possibility of gating. Whilst this is not important in the present case—the channel length is 2 μm and the overall conductance of the device is controlled by the behavior at the contacts—gating should become increasingly effective as the channel

length is reduced, allowing modulation of the tails in the barriers that extend into the channel from the electrode regions on either side.

CONCLUSIONS

In conclusion, we demonstrate a memristor-diode device in which a population of charged dopants can be created and manipulated. The device exhibits all the hallmarks of a memristor but has the advantage of a well-defined saturated state, a reference to which the device can always be returned. Moreover, the device can be reset into an off-state that is well defined with respect to the saturated state and from which its conductance can be controllably evolved into a precision multilevel memory.

METHODS

Single nanowire devices are fabricated following a three step process of UV lithography that involves defining contact pads, nanowire spray deposition, and electron beam lithography (EBL) to define metal contacts to the wires. Devices were fabricated on silicon substrates with 200 nm oxide thickness. UV lithography was used to produce 150 µm2 Ti/Au metal contact pads with thickness 5/30 nm, respectively. Dilute solutions of commercially available TiO_2 wires (EMFUTUR) dispersed in deionized water were then hand-sprayed onto the substrate. EBL was used to draw Au metal contacts 80 nm thick to each individual nanowire such that only Au metal was in contact with the wires. The physical dimensions of the TiO_2 nanowires are between 50-100 nm in diameter and 5-20 µm in length. Transmission electron microscopy confirmed the crystallographic structure of the single crystal anatase TiO_2 nanowires (see Supporting Information Figure S1).

Electrical measurements were performed on the single nanowire devices using a 2-point probe setup with a Keithley 4200-SCS parameter analyzer. Electroforming steps were carried out by applying 10 V with a 1 nA compliance for approximately 103 seconds. Typical triangle wave voltage sweeps were performed at a sweep rate of 0.23 V/s with a magnitude of 10V. Frequency dependence was investigated by varying the sweep delay between points that comprise a 20 point triangle wave voltage pulse. Very low frequency AC impedance measurements were carried out as prescribed by the VLF C-V application note and involved the application of a 350 mV AC modulation at 10 Hz.[29]
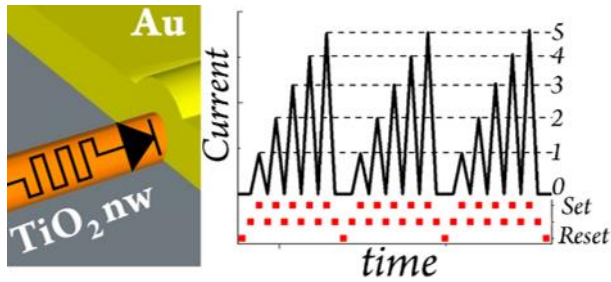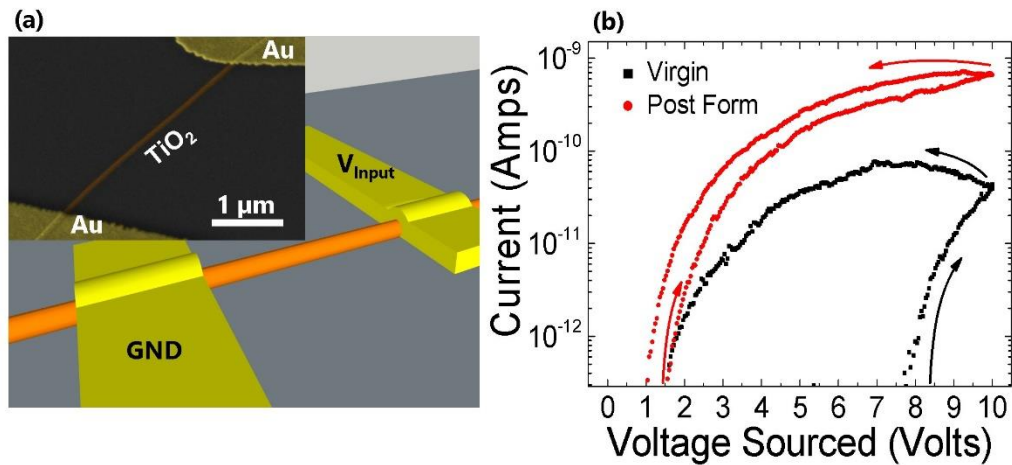
Figures and Captions.

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Figure 1. (a) A schematic of a typical nanowire device showing a single TiO$_2$ nanowire spanning two Au metal contact pads. Inset is an electron microscope image of a typical TiO$_2$ nanowire junction device. (b) The response of a virgin single TiO$_2$ nanowire device to a 10 V voltage sweep both before and after carrying out a +10 V forming step on the wire. The device is shown to be more conductive after the forming step has been carried out.
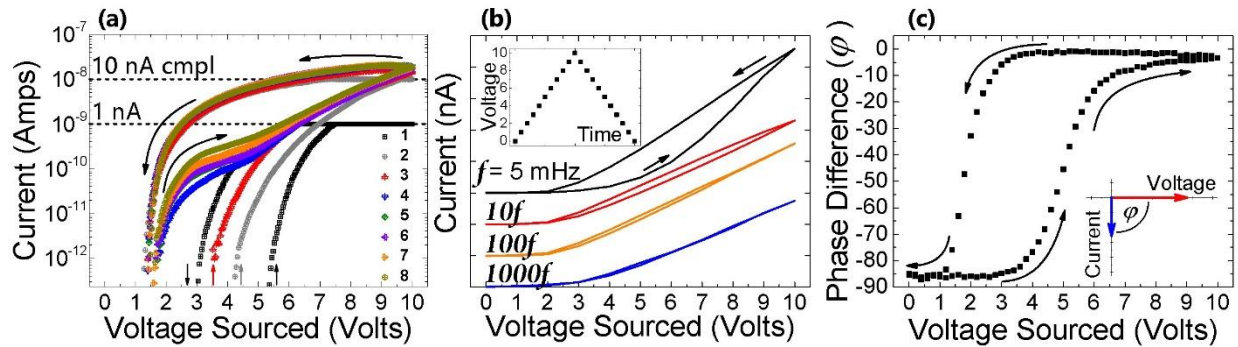
Figure 2.   Many properties of a memristor depend heavily on the electrical stimulus and the device history. In (a) the evolution of the current response of the nanowire device to the same voltage pulse is shown for a sequence of 8 pulses performed directly after each other. The first and second voltage sweeps hit 1 nA and 10 nA compliances respectively; each subsequent sweep increases the maximum current within the device until a pseudo-steady-state saturation point is reached whereby the current is no longer changing. This saturation point was used as a point of reference for further experiments. (b) As the frequency of the applied voltage sweep increases, the current at saturation for each individual sweep frequency decreases. Hysteresis in the current loop is also observed to decrease with increased sweep frequency. (c) Performing a 10 V DC sweep with a small signal 10 Hz 0.35 V AC component at each point allows the change in device behavior be observed as the sweep progresses. For capacitive circuits the current is -90° out of phase with the driving voltage, thus we observe a dynamic shift from a purely capacitive device to a purely resistive device during the voltage sweep.
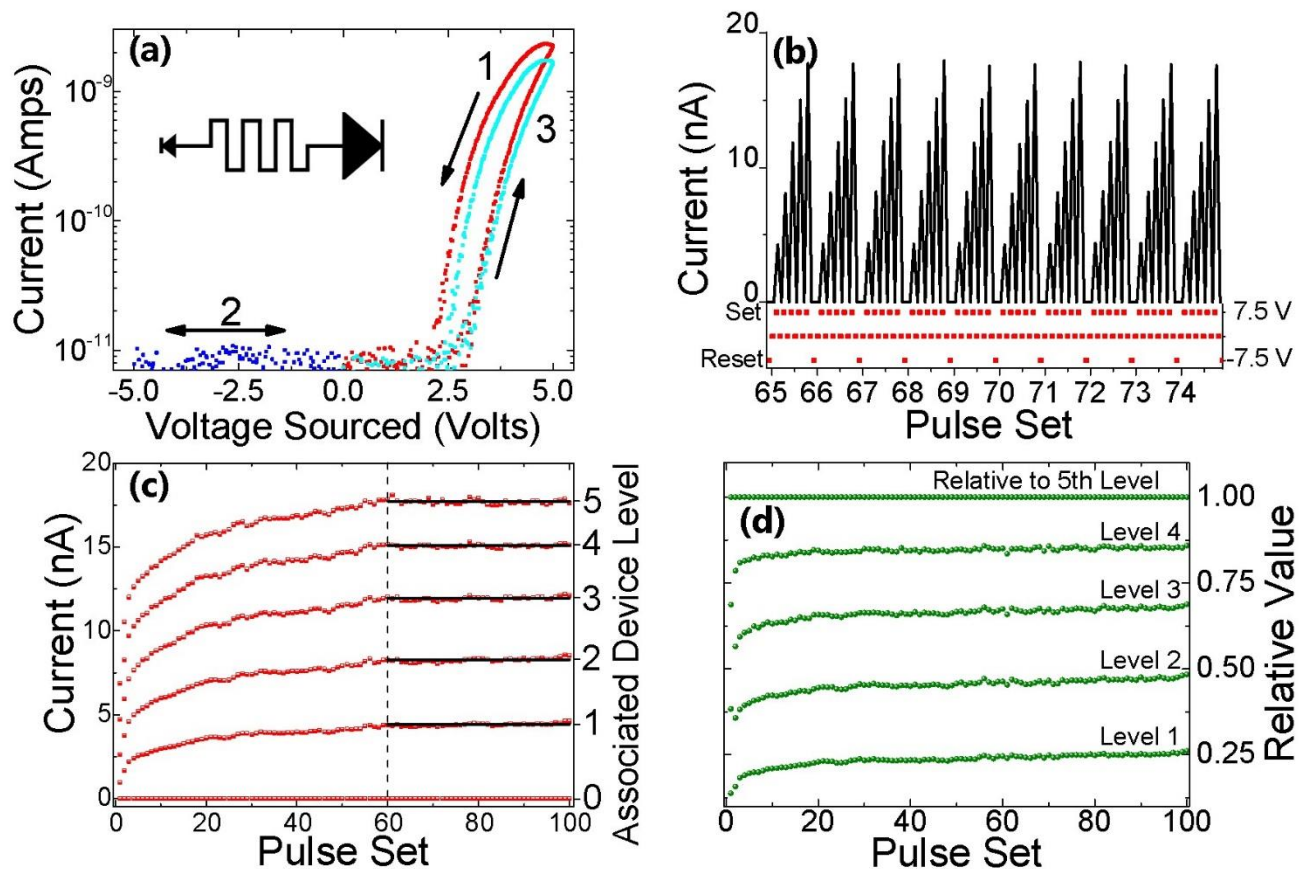
Figure 3. The diode-like behavior of the nanowire junction device is revealed in (a). Current rectification occurs at reverse bias, the degree of which is heavily dependent on the history of applied voltage stimulus. The sequence of voltage stimulus is (1) +5 V forward sweep, (2) -5 V reverse sweep, (3) +5 V forward sweep. Initially saturated at sweep 1, sweep 2 partially erases the saturation state. Sweep 3 is in a less conductive state following sweep 2. (b) It is possible to define arbitrary conductance levels in the device *via* successive pulse applications as shown for a segment involving 5 set voltage pulses (+7.5V). Applying a -7.5V pulse resets the device removing its previous memory: a unique feature of these nanowire junctions. (c) Evolution of the device behavior in (b) during the application of over 100 pulses applied to a nanowire junction. The device conductance levels approach steady state after ~60 pulses and remain within 3% mean value for each memory level. (d) Even during the initial period up to 60 pulse sets of (c), the ratio between the levels remains unchanged relative to the 5th conductance level of each set.
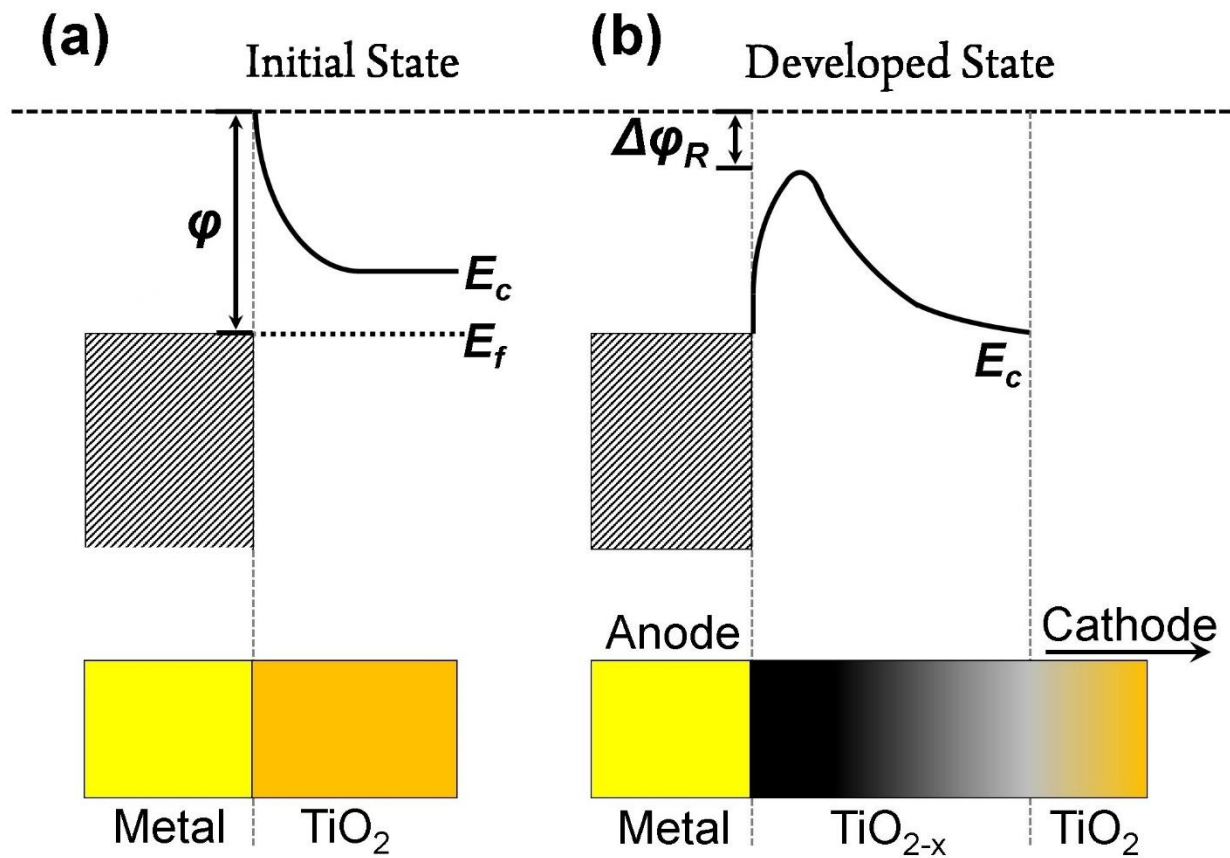
Figure 4.   (a) Band alignment at the contact region of a virgin device, φ is the Schottky barrier height. (b) The Schottky barrier between the TiO_2 wire and the Au electrode has a reduced height and width following the production of a population of oxygen vacancies which act as n-type dopants promoting electrons to the conduction band, $\Delta\varphi_R$ is the reduction in Schottky barrier height. This ultimately increases charge injection and the conductance of the device. Furthermore, this population of dopants is manipulated during device operation giving rise to the dynamic device behavior reported in the text.

AUTHOR INFORMATION

Corresponding Author

*E-mail: jboland@tcd.ie. Phone: +353 1-896-3140.

Supporting Information. High-resolution transmission electron microscopy, selected area electron diffraction, and fast Fourier transforms of the nanowires used in these devices are shown in the supporting information. Device operation under negative bias and a 4 level memory device are also presented along with a comment on device yield. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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