Effective Electrode Length Enhances Electrical Activation of Nanowire Networks: Experiment and Simulation

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ABSTRACT. Networks comprised of randomly oriented overlapping nanowires offer the possibility of simple fabrication on a variety of substrates, in contrast with the precise placement required for devices with single or aligned nanowires. Metal nanowires typically have a coating of surfactant or oxide that prevents aggregation, but also prevents electrical connection. Prohibitively high voltages can be required to electrically activate nanowire networks, and even after activation many nanowire junctions remain non-conducting. Non-electrical activation methods can enhance conductivity but destroy the memristive behavior of the junctions that

comprise the network. We show through both simulation and experiment that electrical stimulation, microstructured electrode geometry, and feature scaling can all be used to manipulate the connectivity and thus, electrical conductivity of networks of silver nanowires with a non-conducting polymer coating. More generally, these results describe a strategy to integrate nanomaterials into controllable, adaptive macroscale materials.

Randomly oriented nanowire networks have the potential to combine novel electronic properties with extreme ease of fabrication.[1, 2] Currently, metallic nanowire networks are being investigated as next-generation transparent conductors,[3, 4] artificial skins,[5-7] and flexible optoelectronic devices.[8-10] However, to build reliable materials and devices, it is necessary to be able to tune the sheet resistance, and hence the connectivity between the wires that comprise these networks. Since most wires are coated with an oxide or some form of surface functionalization, individual junctions between nanowires must be activated, by developing a conducting path between the metallic cores, to allow electrical connectivity between wires.[2] In most instances, these networks are treated post-fabrication to reduce junction resistance as much as possible using heat treatment,[3, 9] mechanical pressure,[11] graphene oxide soldering,[10] and plasmonic welding.[12] However, these approaches are not suitable for the vast majority of nanowires due to the presence of a resistive or oxide coating, and even then it is not certain that the lowest possible junction resistances are achieved. Moreover, by attempting to homogenize the junction properties, these approaches erase the emergent electronic behavior that arises from a network of junctions.[13, 14] While the presence of resistive coatings may make maximum conductivity more challenging to achieve, the prospect of controlling connectivity opens up entirely new device possibilities. In networks where the nanowires themselves have a resistive coating, electrical stressing and the measurement history of the device determine its present

properties. However, for large scale nanowire networks, prohibitively high voltages can be required to activate this memristive behavior,[2, 15] so that the reduction of the activation voltage is an important challenge in realizing large area materials and devices.

Here we show, using both simulation and experiment, that electrode geometry and placement can be manipulated to reduce activation voltage and sheet resistance in a network comprised of silver nanowires with a non-conducting polymer coating. Electrical stressing above a certain activation voltage makes the network conducting by breaking down the polymer in a sufficient number of inter-nanowire junctions to create a current path through the network, and additional electrical stressing causes the network to evolve by adding more current paths, as shown by hysteresis loops in current-voltage measurements.[2] The same nanowire network can demonstrate different electrical behavior at varied network sizes,[2, 16, 17] without tuning the nanowire density in contrast to percolating composites.[18, 19] However, at large electrode separations, large voltages can be required to activate the nanowire network, and the sheet resistances after activation can be high. We show that adding serrations or sharp points to the electrodes lowers the voltage for device activation as well as the overall sheet resistance of the network in current-voltage measurements, due potentially to the creation of localized zones of electric field enhancement compared to flat electrodes and an effective increase in electrode length in contact with the nanowires. Furthermore, we visualize these changes in the network, both experimentally using passive voltage contrast electron microscopy techniques,[20] and in simulations of nanowires as line segments connected in a two-dimensional plane by junctions that can either be capacitive before activation or resistive after activation.[9, 19, 21-24] We compare devices of different electrode geometry: two flat electrodes, one serrated and one flat electrode, two serrated electrodes, and one pointed and one flat electrode. By extending our previously developed model of connectivity

in these networks,[2] we can predict the effects of microstructuring electrodes on the activation voltage and sheet resistance of networks, confirmed here through experimental data. We also discover the importance of electrode length for nanowire networks, and elucidate the role of the overall distributions of junction properties in determining network behavior.

Results and Discussion

Experiment. Silver nanowire network devices were fabricated by spray deposition[25] and evaporation of metal electrodes (see Methods). A transmission electron micrograph of the surface of one silver nanowire is shown in Figure 1(a). The nanowires had mean diameters of 85 ± 10 nm and lengths of 7.5 ± 2 μm, as seen in Figure 1(b), and a 1-2 nm thick coating of polyvinylpyrrolidone (PVP) forming the surface layer, visible in Figure 1(a), which can be non-conducting or conducting depending on the electrical history of the device. Devices were then contacted by probes for electrical measurements, as seen in Figure 2(a) where a nanowire network is bounded by two serrated metal electrodes whose tip-to-tip separation is 200 μm, defining an active network area of 200 μm by 200 μm. Networks are electrically activated by setting the compliance current to either 10 μA or 120 nA depending on device size, then sweeping the voltage to +5 V. The applied voltage selectively breaks down the PVP in junctions with the lowest initial barrier height, and while the exact breakdown mechanism is not known, network activation still occurs when samples are contacted in vacuum, implying that polymer breakdown does not depend on environment. The breakdown of the PVP creates cells of electrical connectivity within the device, and these cells grow in size and ultimately connect to form a conducting path through the network until current compliance is reached.[2] The voltage at which this initial activation occurs is recorded as V_{on}. In the experiments reported here, a 50 μm

by 50 μm nanowire network was contacted either by two flat electrodes, a single flat electrode and a pointed electrode, a single flat electrode and a single serrated electrode, and two serrated electrodes, as shown schematically in Figure 2(b).

Current-voltage (I-V) measurements were performed by increasing the current compliance to 5 mA after activation, and the voltage is swept from 0 to $+V_{max}$ to 0 to $-V_{max}$. Initially V_{max} is set to V_{on}. Then the maximum voltage is gradually increased, to activate additional current paths, evolving the network. Sample activation and evolution I-V curves for a device, as well as an electron micrograph of the nanowire network for the case of point and bar electrodes separated by 50 μm, are shown in Figure 3. Sheet resistance is measured immediately after device activation when current is stable, and these measurements are performed over a sufficiently low voltage range so that additional evolution does not occur and the resistance is stable. Based on four-probe measurements, for a 50 μm by 50 μm nanowire network we would expect ~65% of the resistance to come from the contact between the electrodes and the nanowire network, with the remaining resistance coming from the nanowires and interwire junctions. All four geometries were then compared by examining the V_{on} and sheet resistance at V_{on} of each device.

To quantitatively compare electrical behavior of different electrode geometries, we compare averaged results from 6 flat electrode devices and 4 doubly serrated electrode devices from the same Ag nanowire network. We find that for the flat electrode devices, V_{on} = 1.97 V and R (V_{on}) = 4800 Ω and, and for doubly serrated electrode devices, V_{on} = 1.18 V and R (V_{on}) = 3600 Ω. The average experimental error in R is ~30% and in V_{on} is ~20% due to random variation in the network properties. Thus serrations reduce R to 0.74 times its value for the square electrode case, and reduce V_{on} to 0.60 times its value for the square electrode case. The results for ~30 total

devices from multiple chips are tabulated in Table 1. Each number is the ratio between the performance values of devices with more complex electrode geometries (one electrode serrated, both electrodes serrated, or one electrode pointed) and the performance values of a flat square electrode shape. The tabulated data show that, on average, serrations strongly reduce V_{on} and sheet resistance. Passive voltage contrast imaging in a scanning electron microscope shows that the serrations or points on the electrode are preferentially activated as in Figure 4, where part (a) shows topography, and part (b) shows passive voltage contrast imaging of connected nanowires. Note in (b) the darker, less visible regions of the network form a conducting path between the electrodes, whereas the brighter wires are disconnected from this path but can become connected after additional electrical stressing.[2] The data from the point and bar geometry show the largest scatter, which we suggest is due to the increased importance of a single area of the nanowire network (*i.e.* at the point), compared to serrations which have several possible nucleation sites for conductivity pathways. The large numbers of devices measured on two different chips indicate that these results are very reproducible. We performed the same set of measurements for 200 μm square networks, and found similar reductions in V_{on} but a smaller reduction in sheet resistance (see Supporting Information for expanded data tables). We attribute this behavior to the fraction of wires in the device that contribute to the formation of the conducting path. For the smaller 50 μm gaps, the fraction of wires that are in the conducting path is larger, and the areas of enhanced electric field constitute a larger percentage of the total device area. We also examined rectangular electrodes with the same inter-electrode spacing but twice the electrode length, to see if the additional electrode length by itself, without structuring to induce field enhancement, would reduce sheet resistance. We observed reductions of 10-50% for the flat

rectangular electrodes compared to the flat square case strongly suggesting that the increased electrode length is likely the main factor in reducing the sheet resistance.

Simulation. Whilst we can propose qualitative explanations for the geometric scaling effects on the electrical behavior, we also performed simulations of static electric properties to corroborate these results and obtain physical insights about the nanowire network properties and their dependence on junction properties. In our model of network activation, the nanowires are represented by one-dimensional rods lying on a two-dimensional plane.[21] Their length l_w, center point position (x_c,y_c) and angle θ are randomly generated in order to create randomly-oriented networks. When a bias voltage V is applied across the network, individual voltage drops v_i occur across each junction i, with the wires treated as equipotential line segments. The inter-nanowire junctions can be either non-activated, if the voltage drop v_i across the junction is not strong enough to modify the dielectric coating, or activated, if $v_i \geq v_{b_i}$, where v_{b_i} is the voltage drop across junction i above which the dielectric is modified so that a conducting path forms between the nanowires. The non-activated junctions can be described as capacitors, building up charge on both sides of the dielectric coating, and the activated junctions can be described as resistors, with resistance determined by the conducting path that links the metallic cores. In fact, we consider the junction resistances to be the only source of resistance in the model, thus the resistance of the junctions dominates the overall network resistance. In this representation, the junction break voltage v_{b_i} represents the junction voltage above which the junction behavior switches from capacitive to resistive. Therefore, as one increases the applied voltage, the system reaches activation ($V = V_{on}$) when there is a percolating path of resistors. The physical characterization of the network is based on individual wire lengths and network junction properties—resistances R_i, capacitances C_i and break voltages—taken from random distributions generated from

experimental measurements on individual junctions. The electrical properties of the nanowire networks can then be described using Ohm's law and Kirchoff's circuit laws, similar to the approach developed by Cserti.[26] These laws can be summarized in the following equation:

$$I_j = \sum_{<l,j>} \frac{U_j - U_l}{R_{jl}}, \tag{1}$$

where U_j is the electrostatic potential at wire j, R_{jl} is the resistance at the junction between wires j and l, I_j is the current going in or coming out of wire j and the sum is on l, where l is the first nearest neighbor (FNN) of j. This equation can be written in matrix notation as

$$\mathbf{M}_R \mathbf{U} = \mathbf{I}, \tag{2}$$

where **U** contains the potential at each wire and **I** represents the current that goes in and out of each element (nanowire or electrode) of the network circuit. **I** is a vector with only two non-zero values (i and $-i$), corresponding to the source and drain elements, and zero values for all the remaining wires. Furthermore, the matrix $\mathbf{M}_R$, which contains the system connectivity, is defined as

$$M_R^{jl} = \begin{cases} \sum_{<k,j>} R_{jk}^{-1}, \text{if } j = l \\ -R_{jl}^{-1}, \text{if } j \text{ and } l \text{ are FNN} \\ 0, \text{if otherwise} \end{cases}. \tag{3}$$

After solving equation (2) for **U**, one can obtain the system conductance from

$$\Gamma_{LR} = R_{LR}^{-1} = \left(\frac{U_L - U_R}{i}\right)^{-1}, \tag{4}$$

where L and R represent the left and right leads respectively.

Before calculating the capacitance, one must determine which junctions are activated by solving a matrix equation based on the definition of the capacitance, $C = Q/V$,

$$\mathbf{M}_C\mathbf{U} = \mathbf{Q}\,, \tag{5}$$

where $\mathbf{M}_C$ has the same form as $\mathbf{M}_R$ exchanging R_{jl}^{-1} for C_{jl}. $\mathbf{Q}$ represents the charge that builds up on the system due to the applied voltage V. If one solves this equation for $\mathbf{U}$, the v_i across any junction can be determined for any voltage applied to the network. Therefore, only the activated junctions will be considered when determining $\mathbf{M}_R$.

In the present model, we add charge accumulation at the sharp edges of the contacts, as a proxy for the electric field enhancement due to the electrode geometry. The aim is to understand how the enhancement in the network connectivity due to this effect compares to the enhancement that originates from the increase of the electrodes effective length. The distributions of junction resistance, junction capacitance, junction activation voltage, and nanowire length were generated from experimental measurements on single nanowire-nanowire junctions, as well as the experimentally measured nanowire density and network size. (See the Supporting Information for the junction property distributions used.) We found gamma distributions based around experimental mean values to give the best agreement between experimental and theoretical results, reasonable given that the experimental wire length distribution was itself closest to a gamma distribution. Changing the individual nanowire property distributions affected the final V_{on} and sheet resistance, contrary to previous simulations of one-dimensional memristive networks where the overall network behavior had limited dependence on component memristor properties.[27]

Figure 5 shows the connectivity paths that form as the simulated voltage across the network is increased. There is a clear difference between the activation patterns in the four cases, with some paths seeded by serrations and more paths coming from microstructured electrodes. In our simulations, the change in V_{on} and sheet resistance is mainly due to the increase in electrode length, and our results show that charge accumulation and field enhancement plays only a very minor role in the improvement of the connectivity on the length scales employed in the present experiments. Even increasing the tip angle to 30°, which should enhance the electric field further, had a negligible effect on V_{on}, implying that the most important change in connectivity comes from differences in the effective electrode length between the four cases presented. The left panels of Figure 5 show the wires that form conducting paths to the left (in green) and right (in red) electrodes when the network is under an applied voltage of $0.66V_{on}$, for various electrode geometries. Under these conditions there is no continuous conducting path between the electrodes. The center panels show the wires (in blue) which have just formed conducting paths connecting both electrodes, meaning that the system has achieved a percolating path of resistors and the conductance becomes non-zero, at $V = V_{on}$. The right panels show the evolution in the conducting paths (in blue) in the network when the voltage is increased to $1.33V_{on}$. The actual voltages are shown in Figure 5 for each of the four electrode configurations.

Simulations show that junction activation begins in localized connectivity cells, as found in our previous work,[2] and networks became activated when a sufficient number of these cells connect together to establish a conducting path (see Supporting Information for connectivity maps). The number of junctions activated per volt applied initially increases as simulated networks activate, then falls off beyond V_{on}, but in simulations a junction activation fraction approximately equal to 90% was obtained for high voltages, as shown in Figure 6(a). Our results

show that by increasing the network wire density for flat electrodes, the activation voltage and sheet resistance can be continuously reduced, going beyond densities that were implemented experimentally in this work, as shown in Figure 6(b). We examined other electrode geometries at various network densities and found that an increase in network wire density enhances the effect of increasing the effective electrode length, enabling easier network activation. It is worth noting, however, that increasing the network wire density reduces the system transparency which is an important issue for transparent conductor applications. Furthermore, in simulated devices whose electrode width is twice as large as the inter-electrode separation, V_{on} is lowered by 13% compared with the square network case, confirming our experimental measurement that increasing electrode length without electric field enhancement modifies device behavior.

Table 1 summarizes the experimental and simulated resistance and V_{on} values for the four combinations of electrode geometries. Comparing these results, one sees that our simulation model underestimates the reduction in V_{on} generated by microstructuring the electrodes. Nevertheless, the simulations consistently predict an improvement of the network connectivity from designing electrodes with sharp features. One possible explanation for the discrepancy between the magnitudes of the changes in V_{on} and sheet resistance shown experimentally and predicted by simulation is aging of the junctions themselves. Following the initial polymer breakdown in a single junction which marks activation of that junction, the resistivity can continue to change as the whole network is electrically stressed. The strength of the junction connection may deepen, and this behavior is not accounted for in our simulations because it is not physically well understood. Also, our simulations used constrained nanowire networks in which wires outside the device area are not considered, while in experiments we know from passive voltage contrast imaging that some connectivity paths may evolve around the edges of

the device area, and these additional paths may increase the impact of electrode microstructuring. However, in general, simulations and experiments both demonstrate that electrode geometry can be used as a handle to tune nanowire network behavior, in addition to the more obvious methods of changing the density of nanowires and the distribution of wire properties.

Conclusion

In both experiments and simulations, we find that the increased effective length associated with microstructured electrodes results in modifications of the electrical device behavior within the same nanowire network. Reductions of 10-40% are observed in the activation voltage and sheet resistance, with the strongest reductions both predicted and measured for devices with two serrated electrodes. Simulated networks of nanowires show that the distribution of nanowire properties is critical to the final network behavior, and that electrode length is a much larger factor than electric field enhancement in changing network behavior. By using electrical stressing, microstructure of electrodes, and feature scaling, we can tune the connectivity and conductivity of these nanowire networks to sidestep previous limitations of high activation voltage and high sheet resistance. Electrode microstructure is a facile route to controlled activation and memristive behavior in nanowire network devices. For any given nanowire network, the electrical properties can be tuned by choosing electrode separation and geometry, thus allowing the electrical behavior of the nanowire network to be optimized for the desired application. The programmable properties that emerge from individual junction behavior can then be controlled and used for applications such as neuromorphic electronics, artificial skin, and transparent conductors. Our combined experimental and theoretical results demonstrate the emergent physics of how nanoscale materials such as silver nanowire networks can be electrically connected and controlled to develop adaptive macroscopic nanostructured materials.

Additional refinement of the model by incorporating electric field effects within the network and nuanced evolution of junctions will assist in future combined experimental and computational work.

METHODS.

Devices were fabricated on silicon wafers coated with 300 nm of thermal silicon oxide. Silver nanowires obtained from Seashell Technologies were spray-deposited onto the substrates, using an Infinity Spray Gun mounted in a Janome JR 2300N Desktop Robot for evenly dispersed and randomly oriented sprayed networks. Electron beam evaporation was then used to deposit 5 nm of titanium as an adhesion layer, followed by 60 nm of gold, through a shadow mask to define electrical contacts. The top-contacted electrodes ensure good electrical connection to the nanowires, which were sprayed to a density of 0.3 nanowires/μm^2 or 85% transmittance. Nanowire size distributions were measured by examining scanning electron micrographs by hand in ImageJ. Electrical measurements were performed by contacting the two lateral electrodes with probes connected to a computer-controlled voltage source (Keithley 2400) to record current-voltage (I-V) characteristics for each device. Transmission electron microscopy was performed on an FEI Titan, and scanning electron microscopy was performed on a Zeiss Ultra. Simulations were written in Python.

FIGURE CAPTIONS.

Figure 1. (a) Transmission electron micrograph showing a silver nanowire with non-conducting polymer surface coating visible. (b) Length distribution for silver nanowires used. The mean value and asymmetric shape were used as a basis for simulation nanowire length distributions.

Figure 2. (a) Scanning electron micrograph showing a 200 μm silver nanowire network device between two serrated metal electrodes, contacted by two sharp probes for electrical measurement and imaging. (b) Diagram showing all of the electrode geometries explored in this study. Electrodes can either be square and flat on all sides, or have one side serrated, or both sides serrated, or have one side come to a single point. The electrode shaping affects the total electrode length as well as the electric field strength in the device area.

Figure 3. (a) Scanning electron micrograph for a 50 μm silver nanowire network device with one pointed electrode. The 60° point enhances the electric field for a given applied voltage, but only in a small region of the nanowire network. (b) Current-voltage characteristics for the same device. The inset shows activation occurring at an activation voltage of 0.75 V, with a set current compliance of 120 nA. Evolution of the sheet resistance occurs on subsequent electrical sweeps as shown in the main graph. The initial sheet resistance can be calculated by examining the measured current, without compliance, at the activation voltage, and compared between devices with shaped electrodes and devices with flat electrodes.

Figure 4. (a) Secondary electron image showing topography of a 50 μm silver nanowire network device with one serrated electrode. (b) Scanning electron micrograph with passive voltage contrast from an in-lens detector of the same device as in (a). The device has been electrically activated and the darker nanowires are connected to ground, showing conductivity paths seeded by the serrations.

Figure 5. Simulated activation for nanowire networks with a density of 0.3 nanowires/μm^2 between (a) flat electrodes, (b) one flat and one serrated electrode, (c) two serrated electrodes, and (d) point and bar electrodes. The left, center and right panels show the networks at $V = 0.66V_{on}$, $V = V_{on}$ and $V = 1.33V_{on}$, respectively. The dark gray areas represent the electrodes. The red, green and blue wires belong to conducting paths to left, right and both electrodes, respectively.

Figure 6. (a) Simulated ratio of activated junctions to total junctions f_a as a function of the applied voltage V for a 200 x 200 μm network with flat electrodes (V_{on} = 15 V) and a nanowire density of 0.3 nanowires/μm^2. The inset shows the same curve as the main plot for lower voltage values. (b) Simulated activation voltage V_{on} and sheet resistance at activation R_{on} as a function of wire density for the flat electrode case.

TABLES.

Electrode Geometry	Relative Experimental Resistance	Relative Simulated Resistance	Relative Experimental V_{on}	Relative Simulated V_{on}	Effective Electrode Length
Flat	1.00	1.00	1.00	1.00	1.00
Single Serrated	0.78	0.99	0.88	0.86	1.43
Double Serrated	0.74	1.03	0.60	0.82	1.86
Point and Bar	0.72	1.01	0.68	0.94	1.43

Table 1. Comparison of experimental and simulated sheet resistance, experimental and simulated activation voltage, and electrode length for nanowire network devices with various sizes and electrode geometries. The nanowire density for all devices was 0.3 nanowires/μm^2. Each entry is a ratio of the change between the value for a shaped electrode and the value for a flat electrode, so that the flat electrode ratios are all 1.

ASSOCIATED CONTENT

Supporting Information. Data tables of activation voltage and sheet resistance; distributions of resistance, capacitance, and voltage break values used for junction simulations, and simulated junction activation map for a large network. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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Author Contributions

J.A.F. wrote the paper, performed the nanowire network measurements, and did the scanning electron microscopy and sample fabrication. C.R. performed network simulations and modelling. A.T.B. provided single-junction values. E.K.M. performed transmission electron microscopy. M.S.F. developed the model, and M.S.F. and J.J.B. directed the work.

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REFERENCES

1. Madaria, A. R.; Kumar, A.; Ishikawa, F. N.; Zhou, C., Uniform, Highly Conductive, and Patterned Transparent Films of a Percolating Silver Nanowire Network on Rigid and Flexible Substrates Using a Dry Transfer Technique. *Nano Res.* 2010, 3, 564-573.
2. Nirmalraj, P. N.; Bellew, A. T.; Bell, A. P.; Fairfield, J. A.; McCarthy, E. K.; O'Kelly, C.; Pereira, L. F. C.; Sorel, S.; Morosan, D.; Coleman, J. N.*, et al.*, Manipulating Connectivity and Electrical Conductivity in Metallic Nanowire Networks. *Nano Lett.* 2012, 12, 5966-5971.

3. De, S.; Higgins, T. M.; Lyons, P. E.; Doherty, E. M.; Nirmalraj, P. N.; Blau, W. J.; Boland, J. J.; Coleman, J. N., Silver Nanowire Networks as Flexible, Transparent, Conducting Films: Extremely High DC to Optical Conductivity Ratios. *ACS Nano* 2009, 3, 1767-1774.
4. Yim, J. H.; Joe, S.-Y.; Pang, C.; Lee, K. M.; Jeong, H.; Park, J.-Y.; Ahn, Y. H.; de Mello, J. C.; Lee, S., Fully Solution-Processed Semitransparent Organic Solar Cells with a Silver Nanowire Cathode and a Conducting Polymer Anode. *ACS Nano* 2014, 8, 2857-2863.
5. Boland, J. J., Flexible Electronics: Within Touch of Artificial Skin. *Nat. Mater.* 2010, 9, 790-792.
6. Gong, C.; Liang, J.; Hu, W.; Niu, X.; Ma, S.; Hahn, H. T.; Pei, Q., A Healable, Semitransparent Silver Nanowire-Polymer Composite Conductor. *Adv. Mater.* 2013, 25, 4186-4191.
7. Takei, K.; Takahashi, T.; Ho, J. C.; Ko, H.; Gillies, A. G.; Leu, P. W.; Fearing, R. S.; Javey, A., Nanowire Active-Matrix Circuitry for Low-Voltage Macroscale Artificial Skin. *Nat. Mater.* 2010, 9, 821-826.
8. Lan, X.; Bai, J.; Masala, S.; Thon, S. M.; Ren, Y.; Kramer, I. J.; Hoogland, S.; Simchi, A.; Koleilat, G. I.; Paz-Soldan, D*., et al.*, Self-Assembled, Nanowire Network Electrodes for Depleted Bulk Heterojunction Solar Cells (Adv. Mater. 12/2013). *Adv. Mater.* 2013, 25, 1768-1768.
9. Langley, D. P.; Giusti, G.; Lagrange, M.; Collins, R.; Jiménez, C.; Bréchet, Y.; Bellet, D., Silver Nanowire Networks: Physical Properties and Potential Integration in Solar Cells. *Sol. Energ. Mat. Sol. Cells* 2014, 125, 318-324.
10. Liang, J.; Li, L.; Tong, K.; Ren, Z.; Hu, W.; Niu, X.; Chen, Y.; Pei, Q., Silver Nanowire Percolation Network Soldered with Graphene Oxide at Room Temperature and Its Application for Fully Stretchable Polymer Light-Emitting Diodes. *ACS Nano* 2014.
11. Hu, L.; Kim, H. S.; Lee, J.-Y.; Peumans, P.; Cui, Y., Scalable Coating and Properties of Transparent, Flexible, Silver Nanowire Electrodes. *ACS Nano* 2010, 4, 2955-2963.
12. Garnett, E. C.; Cai, W.; Cha, J. J.; Mahmood, F.; Connor, S. T.; Greyson Christoforo, M.; Cui, Y.; McGehee, M. D.; Brongersma, M. L., Self-Limited Plasmonic Welding of Silver Nanowire Junctions. *Nat. Mater.* 2012, 11, 241-249.
13. Avizienis, A. V.; Sillin, H. O.; Martin-Olmos, C.; Shieh, H. H.; Aono, M.; Stieg, A. Z.; Gimzewski, J. K., Neuromorphic Atomic Switch Networks. *PLOS ONE* 2012, 7, e42772.
14. Oskoee, E. N.; Sahimi, M., Electric Currents in Networks of Interconnected Memristors. *Phys. Rev. E: Stat., Nonlinear, Soft Matter Phys.* 2011, 83, 031105.
15. Yang, J. J.; Strukov, D. B.; Stewart, D. R., Memristive Devices for Computing. *Nat. Nanotechnol.* 2013, 8, 13-24.
16. Bellew, A. T.; Bell, A. P.; McCarthy, E. K.; Fairfield, J. A.; Boland, J. J., Programmability of Nanowire Networks. *Nanoscale* 2014.
17. Mutiso, R. M.; Kikkawa, J. M.; Winey, K. I., Resistive Switching in Silver/Polystyrene/Silver Nano-Gap Devices. *Appl. Phys. Lett.* 2013, 103, 223302-1-5.
18. Bergin, S. M.; Chen, Y.-H.; Rathmell, A. R.; Charbonneau, P.; Li, Z.-Y.; Wiley, B. J., The Effect of Nanowire Length and Diameter on the Properties of Transparent, Conducting Nanowire Films. *Nanoscale* 2012, 4, 1996-2004.
19. White, S. I.; Mutiso, R. M.; Vora, P. M.; Jahnke, D.; Hsu, S.; Kikkawa, J. M.; Li, J.; Fischer, J. E.; Winey, K. I., Electrical Percolation Behavior in Silver Nanowire–Polystyrene Composites: Simulation and Experiment. *Adv. Funct. Mater.* 2010, 20, 2709-2716.

20. Colvin, J., A New Technique to Rapidly Identify Low Level Gate Oxide Leakage in Field Effect Semiconductors Using a Scanning Electron Microscope. *EOS/ESD Symp. Proc.* 1990, EOS-12, 173-174.
21. Li, J.; Zhang, S.-L., Finite-Size Scaling in Stick Percolation. *Phys. Rev. E: Stat., Nonlinear, Soft Matter Phys.* 2009, 80, 040104.
22. Mutiso, R. M.; Sherrott, M. C.; Rathmell, A. R.; Wiley, B. J.; Winey, K. I., Integrating Simulations and Experiments To Predict Sheet Resistance and Optical Transmittance in Nanowire Films for Transparent Conductors. *ACS Nano* 2013, 7, 7654-7663.
23. Obukhov, S. P., Percolation in a System of Randomly Distributed Sticks. *J. Phys. A: Math. Gen.* 1988, 21, 3975-3978.
24. Žeželj, M.; Stanković, I., From Percolating to Dense Random Stick Networks: Conductivity Model Investigation. *Phys. Rev. B* 2012, 86, 134202.
25. Scardaci, V.; Coull, R.; Lyons, P. E.; Rickard, D.; Coleman, J. N., Spray Deposition of Highly Transparent, Low-Resistance Networks of Silver Nanowires over Large Areas. *Small* 2011, 7, 2621-2628.
26. Cserti, J.; Dávid, G.; Piróth, A., Perturbation of Infinite Networks of Resistors. *Am. J. Phys.* 2002, 70, 153-159.
27. Pershin, Y. V.; Slipko, V. A.; Di Ventra, M., Complex Dynamics and Scale Invariance of One-Dimensional Memristive Networks. *Phys. Rev. E: Stat., Nonlinear, Soft Matter Phys.* 2013, 87, 022116.