Resistance of Single Ag Nanowire Junctions and their Role in the Conductivity of Nanowire Networks

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ABSTRACT: Networks of silver nanowires appear set to replace expensive indium tin oxide as the transparent conducting electrode material in next generation devices. The success of this approach depends on optimising the material conductivity, which up to now has largely focused on minimising the junction resistance between wires. However, there have been no detailed reports on what the junction resistance is, nor is there a known benchmark for the minimum attainable sheet resistance of an optimised network. In this paper we present junction resistance measurements of individual silver nanowire junctions, producing for the first time a distribution of junction resistance values, and conclusively demonstrating that the junction contribution to the overall resistance can be reduced beyond that of the wires themselves through standard processing techniques. We

find that this distribution shows the presence of a small percentage (6%) of high-resistance junctions, and we show how these may impact the performance of network-based materials. Finally, through combining experiment with a rigorous model, we demonstrate the important role played by the network skeleton and the specific connectivity of the network in determining network performance.

KEYWORDS: silver, nanowire, junction, network, resistance, transparent, conductor

TEXT:

The advanced electronics market continues to demand thinner and more powerful devices such as smart phones, tablets, flat-screens etc. If current trends continue, flexible device platforms will dominate the marketplace in the coming decades. To enable this transition, flexible, transparent, conducting thin films are necessary to facilitate the capacitive touch screen technology that will inevitably be required in such platforms. The current market leader, ITO (tin-doped indium oxide), is very brittle and thus not suitable for these future device technologies. Several alternatives to ITO have emerged in the past decade, and include conductive polymers,[1] graphene,[2-3] networks of metallic nanowires such as Ag, Au, and Cu,[4-9] or composites of these materials incorporating graphene.[10-13] Thus far networks of Ag nanowires have demonstrated the best performance in terms of processing ease, transmittance and electrical conductivity, thereby meeting the requirements for many industrial applications.[14-17]

Early demonstrations of high performance transparent conductors made from Ag nanowires led researchers to strive to optimise their performance for industrial applications. In this regard many factors have been examined, including the impact of

nanowire geometry,[18-19] the methods used to fabricate the network,[5, 20-23] and the post-fabrication processing techniques employed to remove/modify the insulating polymer shell on the nanowires. The widely used polyol method for Ag nanowire fabrication results in a nanoscale coating of insulting polyvinylpyrrolidone (PVP). Networks fabricated from these nanowires are non-conducting in their native states due to the presence of highly resistive junctions, and post-fabrication processing is required to optimise network conductivity The literature describes different processing techniques to modify the junction properties including thermal annealing,[4, 20-21, 24-25] mechanical pressing,[18, 26] plasmonic welding,[27-28] and most recently a room temperature plasma technique.[14] Despite the intense interest in this area, there is no agreed benchmark for a fully optimised nanowire network. Here, we perform a series of carefully designed measurements to establish the resistance distribution for individual nanowire junctions and incorporate this distribution into a rigorous computational model to accurately predict the properties of a real network. In this manner, we can then draw conclusions about the network's optimisation state, while also examining the role of the junction resistance in determining the network performance.

Junctions are the basic building blocks of any network. It has previously been shown that by controlling the properties of the junction through the use of passivation layers, it is possible to introduce new functionality such as tunable resistance and programmability into an otherwise simple conducting material.[29-30] The junction resistance contribution, R_{jxn}, to the overall sheet resistance of a Ag nanowire network has never been directly measured. Attempts to measure R_{jxn} both directly and indirectly have been inconsistent, with values ranging from just a few ohms to several kilo-ohms being reported.[5, 21, 27, 31-32] Table 1 summarises the values of R_{jxn} reported in the literature to date. It is frequently

assumed that R_{jxn} is significantly larger than the contribution of the nanowires themselves, leading to network models that have omitted the nanowire resistance contribution completely.[31, 33] In instances where individual junction measurements were made, only a single junction was considered so that the values obtained may or may not be representative of the distribution of values in any network. Moreover, not all measurements employed a 4-probe technique, which is necessary to extract accurate resistance values on low impedance metallic nanowire samples. Here we measure for the first time a distribution of junction resistances, obtained through a carefully designed experiment where the resistance of each junction is isolated from the contributions of the individual nanowires. This distribution of values is then combined with a rigorous computational model, producing a realistic simulation of a fully optimised Ag nanowire network.

Table 1. Values of R_{jxn} that have been reported in the literature to date, including the method used.

Author	*Year*	R_{jxn} (Ω)	*Method*
Lee *et al.*[21]	2008	1-100	Fitting simulation to experiment
Hu *et al.*[5]	2010	450	4-probe measurement
Garnett *et al.*[27]	2012	$\sim 1 \times 10^4$	2-probe measurement
Mutiso *et al.*[31]	2013	$\sim 2 \times 10^3$	Fitting simulation to experiment
Song *et al.*[32]	2014	185	2-probe measurement

The nanowires used in this study were purchased from Seashell Technology, and were received coated in a thin (1-2 nm) polymeric layer - a result of the fabrication process (see Figure S2.1 for TEM image). In order to modify this layer and create an ohmic contact between the two wires, the junctions were processed using three different methods: furnace annealing in the absence of oxygen, hot plate annealing under ambient conditions, and electrical activation under ambient conditions via current-induced local heating of the junction – described here as *electroforming*. Each of these methods has been discussed in the literature, and so our results are therefore representative of the average junction behaviour in those reported networks.[21, 25, 32] In the case of furnace annealing, samples were placed into a tube furnace at 200°C under dry N_2 flow for 2 hrs, whilst hotplate annealing was performed at 180°C for 2 min in air. For both furnace- and hotplate-processed samples, contacting with electron beam lithography (EBL) defined electrodes was performed after the anneal step.

Prior to any junction resistance measurement it is essential to ensure that the four electrical contacts (two on either side) make good electrical contact with their respective wires (see Figure 1a, inset). Typically we find that there is a low resistance contact to each nanowire, which is likely the result of the large heat of condensation released during metal contact formation. If this is not the case these contacts need to be activated separately by driving current between electrodes 1-2 and 3-4. The next step involves activation of the junction itself. This must be performed using two contacts instead of four, as the resistance of the inner circuit in a 4-probe set-up is lower than that of the nanowire junction prior to activation. The insulating PVP layer prevents current flow up to a threshold, V_{FORM}, beyond which the current rises sharply to a pre-defined current compliance level, I_{CC} (see Figure 1b). This process is directly analogous to the

electroforming process used to generate the initial conductive state in resistive switching materials.[34]

Once the junction had been activated the resistance level was measured. If the resistance remained high (> 500 Ω), further current was driven through the junction, generating significant local Joule heating at the junction which in most instances resulted in a further reduction of the junction resistance. This additional step was not required in all cases however, and a low I_{CC} of 10 μA was sufficient in some cases to produce an optimised junction. In all cases an optimised junction is defined as a junction whose resistance does not decrease further following additional thermal and/or electrical processing. The effectiveness of this current induced anneal to improve the resistance is illustrated in Figure 1c as the resistance of the junction shown in Figure 1a is reduced from 507 Ω to just 30 Ω post processing at a maximum drive current of 5 mA.

Measuring the junction resistance

Once the junctions were optimised, the resistance contributions from the external circuit and the nanowire/metal contact resistances were identified and removed from the measurement through the 4-probe technique. A maximum current of 50 μA was driven through all thermally optimised junctions *i.e.* furnace or hotplate processed, so that even these junctions experienced a significant electrical stress. However no change in resistance beyond the thermally optimised value was found, indicating the effectiveness of thermal processing methods. The recovered resistance can be described as a linear series of resistors, R1, R2, and R_{jxn} as shown in Figure 2a, where R1 and R2 are the resistance contributions of nanowire 1 and 2, respectively. R1 and R2 are evaluated by

measuring the dimensions of each nanowire (SEM), where L was measured from the outside of the inner contact electrode to the centre of the nanowire junction (see Figure 2b) as described by Kolesnik *et al.*[35] The resistivity value used to calculate R1 and R2 was determined by performing 4-probe measurements on almost 40 individual nanowires, with diameters ranging from 50 to 90 nm, and resulted in an average resistivity of 20.3 ± 5.5 nΩ.m. This value is quite close to that of bulk silver (15.9 nΩ.m), and is consistent with values previously measured by Huang *et al.* for single crystal Ag nanowires.[36] No dependence of the resistivity on nanowire diameter was observed for the nanowires measured - see Supporting Information for more information. This resistivity value was then used to estimate R1 and R2, and to extract values for R_{jxn}.

The junction resistance was determined for Ag nanowires processed using the three methods described above. Figure 3a plots the calculated R_{jxn} value as a function of frequency (bin size of 10 Ω) for each of these methods, designated in varying shades of grey. The distribution shows a strong peak at 11 Ω, corresponding to the median value of the distribution (red dash line). The negative values reported in Figure 3a arise from the separate estimates of R1 and R2 relative to the measured resistance, and can be accounted for by the calculated error. We note that junctions representative of all three processing methods are found across the distribution, indicating that within the limits of our experiment the different processing methods produce junctions of equally low resistance values. Moreover these junction resistance values are, to our knowledge, the lowest measured values ever reported. We also note the presence of a small quantity of large resistance (200-300 Ω) junctions – the implications of these are discussed below.

To investigate the possible origin of these exceptionally low resistance values, SEM analysis was performed on all junctions post-measurement (see Figure 3b-d). It was found

that furnace annealing resulted in near fusing of the wires at the point of contact, forming a welded junction that has been reported previously.[26, 32] In contrast, hotplate annealing and electroforming (Figure 3c-d) result in crossed-wire junctions that appear unmodified by the anneal process, yet have similar junction resistance values compared to fused wires (Figure 3b-d). See Figures S4.1 – S4.3 for additional SEM images. This is surprising since fused wires necessarily have a larger contact area which should result in a reduced resistance. To test whether contact area has an observable effect on junction resistance, the maximum contact area was calculated based on nanowire diameters (see Supporting Information for details), and is plotted against R_{jxn} in Figure 3a, inset. No observable trend is seen, indicating that junction area is not a determining factor on the junction resistance in this case. This result is important, as it implies that junction morphology has very little influence on the resulting resistance. In particular, the welding of two nanowires, a common occurrence during aggressive annealing procedures, appears not to have an appreciable impact on the junction resistance. It is clear that further work is needed to elucidate the reasons behind this finding.

An interesting aspect of the low junction resistances achieved by electroforming is its potential as a route to high conductivity nanowire networks. Compared to alternative processing methods, electroforming is very energy efficient with only relatively low currents (~1 mA) levels required for short durations to produce highly conductive junctions, consistent with earlier experiment and simulations.[29, 32, 36] This agrees with Song *et al.* who showed using finite element simulation that current flow through a nanowire junction results in electromigration of the Ag atoms, thereby improving the contact geometry between the two nanowires.[32] Despite this, it is unlikely that electroforming will lead to optimally conductive networks. While the current driven

through the network will reduce the resistance of the junctions that comprise the percolative conducting paths within it, it will not impact the other sections of the network through which current does not flow, which is expected to be important for large area networks.

These results have additional implications for the optimisation of network materials. Based on the data presented here, it is clear that nanowire-nanowire junctions make a resistance contribution that is comparable or less than the wire segments within the network, *i.e.*, R_{jxn} is approximately equal to the 10 Ω resistance associated with a 1.5 µm length of a 60 nm diameter Ag wire, assuming a bulk Ag resistivity value. It is therefore incorrect to assume, as is often reported in the literature, that junctions are the dominant contributors to the network resistance and future modelling and simulation should account directly for the resistance contribution of the nanowire length segments, in addition to junctions themselves.

Modelling a network and calculating R_s

We now demonstrate the incorporation of the experimental distribution of junction resistance values in Figure 3 into a simulation of a Ag nanowire network. Traditionally, for each network density (number of wires per unit area), simulation involves two types of averaging: one spatial averaging over an ensemble of different wire configurations, and another in which each configuration in turn is averaged over a distribution of possible junction resistance values. To reduce the uncertainties due to averaging we implement a rigorous computational model that does away with the need for the spatial configurational averaging by using a real-world network in which the wire junctions and wire length

segments are mapped to create a near-perfect replica of the original network (see Figure 4). The inter-wire connections are modelled by generating an idealized probability distribution through spline interpolating the data of Figure 3, while the spatial arrangement of the wires remains fixed throughout. The interpolation was performed by setting a minimum cut-off resistance of 0.15 Ω (minimum measured value) and a maximum of 70 Ω. The resistance value of a junction then becomes a random variable that can be chosen given a certain probability defined by the spline distribution. In order to acquire statistical significance for the calculated sheet resistance (R_{calc}), an ensemble of junction resistances is constructed for a respective network with its wires "frozen" at their real micrograph positions. The ensembles comprise 25-35 junction resistance sets, depending on the size and density of the system. The calculated mean (R_{calc}) and error in the sheet resistance are determined and compared to the experimentally observed value (R_{exp}). The model accounts for both junction and intra-wire resistance contribution, and as such, a zero value may be attributed to the junction resistances (*i.e.* all junctions are perfect conductors) producing a sheet resistance value, R_0, that is purely due to the resistive contribution of the network skeleton. This provides useful information about the connectivity levels of a network, and can also explain differences in performance seen for seemingly similar networks. Full details about the model used and fabrication of associated networks can be found elsewhere.[37] Details on the nanowire length/diameter statistics are provided in the Supporting Information.

We begin by assuming that the junction resistance values measured between 200 and 300 Ω in Figure 3 represent statistical outliers, and are omitted from the initial calculation. If the experimental and calculated sheet resistance values did not match, these outliers were then introduced gradually into the distribution until the experimental value was reached.

For comparison, both thermally annealed and electroformed networks were modelled. Table 2 lists the measured sheet resistance, R_{exp}, the calculated values, R_{calc} – both with and without the presence of outliers – as well as the percentage of outliers required to bring the numbers into alignment. The skeletal sheet resistance, R_0, nanowire density, and the annealing method used for each network are also included in Table 2. We find that the distribution of junction values peaked around 11 Ω consistently yields a sheet resistance (R_{calc}) that is within 10 Ω of the experimentally determined values (R_{exp}). Given the complexity of these systems this is a remarkable result, and shows that it is possible to accurately calculate the resistance of any Ag nanowire network, and that the junction resistance values reported here are representative of those that exist within actual networks.

Table 2. Experimental sheet resistance values (R_{exp}) of six distinct 20 x 20 μm^2 Ag nanowire networks. The calculated sheet resistance (R_{calc}) for the same network for the case of both zero, and non-zero outlier presence is shown, as is the resistance of the network in the case of $R_{jxn} = 0$ (R_0) – this is the resistance contribution of the nanowire skeleton. The nanowire density and the annealing method used in each case are also included: T = thermal anneal, E = electroform.

Sample	R_{exp} (Ω)	R_0 (Ω)	R_{calc} (Ω) ($n_{out}=0$)	R_{calc} (Ω) ($n_{out}\neq0$)	n_{out} (%)	NW/μm^2	*Anneal Method*
1	77	72	87 ± 4	-	-	0.39	T
2	19	21	26 ± 1	-	-	0.42	T
3	53	34	49 ± 3	53 ± 6	5 ± 1	0.62	T

4	42	32	41 ± 6	-	-	0.35	E
5	37	18	20 ± 1	33 ± 4	34 ± 2	0.36	E
6	66	33	41 ± 5	59 ± 8	27 ± 2	0.39	E

By examining the values of R_0 in Table 2, we can see that the network skeleton contributes a large percentage of the final resistance – on average 80% of R_{calc}. To our knowledge, the contribution from the skeleton has never been specifically accounted for in the optimisation of these materials, yet it represents a fundamental limitation on the performance of these materials and cannot be ignored. Finally, comparing the networks listed in Table 2, it is apparent that the values of R_0 vary significantly even for networks of comparable density (NW/µm^2). As R_0 looks at only the nanowire contribution to the resistance, and not the junctions, this variation must originate from differences in the connectivity patterns within those particular networks, and how efficiently they conduct from one side of the network to the other. Comparing networks 1 and 6 in Table 2, each with a wire density of 0.39 NW/µm^2, we see that a reduction in resistance of over 50% is possible by having a more efficiently connected network (see Figure S6.1 for stick-model images of networks appearing in Table 2). This simple comparison is worth highlighting as it demonstrates the crucial role connectivity plays in determining network performance, and also demonstrates that junction optimisation, while highly influential, is not the only factor controlling performance. Nanowire geometry, in particular nanowire length, is known to impact the resistance of networks by altering the connectivity pathways,[18] but this result demonstrates that controlling the network uniformity is equally

important. Aggregation or clustering of nanowires reduces potential parallel pathways elsewhere, negatively impacting the network resistance. The importance of uniform connectivity is most pronounced in the sparsest networks, for example those needed for high performance transparent conducting applications. Optimising fabrication methods is therefore critical if optimum network performance is to be achieved.

Finally, as was noted earlier, the junction resistance distribution indicates the presence of junctions within networks with resistances that are much higher than the average value. While these high resistance junctions represent only 2 of 32 measured values, or 6.25%, this remains a non-negligible population. It is unclear why these outliers exist and why these junctions cannot be optimised further. Examining Table 2, we see that of the six networks modelled, three required the addition of outliers to bring the R_{calc} values into alignment with R_{exp}; of these, very high outlier quantities were required for the electroformed networks. This is perhaps indicative of poor connectivity within these networks as a result of the electroforming process. We know even low current levels produce low junction resistances, however once a conductive path is formed across the network, the formation of parallel paths is not favoured. This limits the performance of the network, and appears in our model as the presence of high-resistance outliers. This behaviour will likely become amplified in larger networks, and therefore represents a severe limitation of the electroforming technique.

To conclude, in this study we have measured for the first time the resistance distribution for the junction between two Ag nanowires in contact, and have shown that the distribution shows a strong peak at 11 Ω, comparable to the resistance associated with the wire segments within a nanowire network. The accuracy of the distribution was demonstrated by implementing it in a rigorous computational model, and comparing the

experimental and calculated sheet resistances for the same network. It was shown that the model consistently calculates the network resistance within 10 Ω of the experimental value, demonstrating the validity of the resistance distribution for junctions present within a real network. The junction resistance distribution also showed the presence of a finite number of high resistance "outlier" junctions. The origin of these outliers is unknown, however their presence, even at small percentages, has the effect of limiting the ultimate sheet resistance of the film. Another major conclusion of this work is the significant resistance contribution of the network skeleton. This represents a physical limit to the conductivity of these materials, and therefore warrants further exploration. Hopefully this work will motivate and inform the search for fabrication and processing technologies that optimise network connectivity, reduce the presence of "outliers", and ultimately see the full potential of nanowire network based transparent conductors realised.

Experimental Methods

Silver nanowires used in this study were purchased from Seashell Technology, LLC with diameters that varied from 50 to 130 nm (see Figure S1.1). Isolated crossed nanowires (junctions) were prepared by dropping a small volume of a dilute (~ 10 μg/ml) nanowire/isopropanol solution onto clean, thermally grown 300 nm SiO_2 substrates and allowing the alcohol to evaporate in air. Single nanowires and crossed nanowires that formed isolated junctions were then contacted with Ag contact lines, 150 nm in thickness, formed by electron beam lithography and e-beam evaporation. Electrical characterisation was performed using a Keithley 4200 electrical characterisation system. Electron microscopy and electron beam lithography were performed using a Carl Zeiss Supra 40 SEM. Transmission electron microscopy was performed using an FEI Titan TEM.

FIGURES

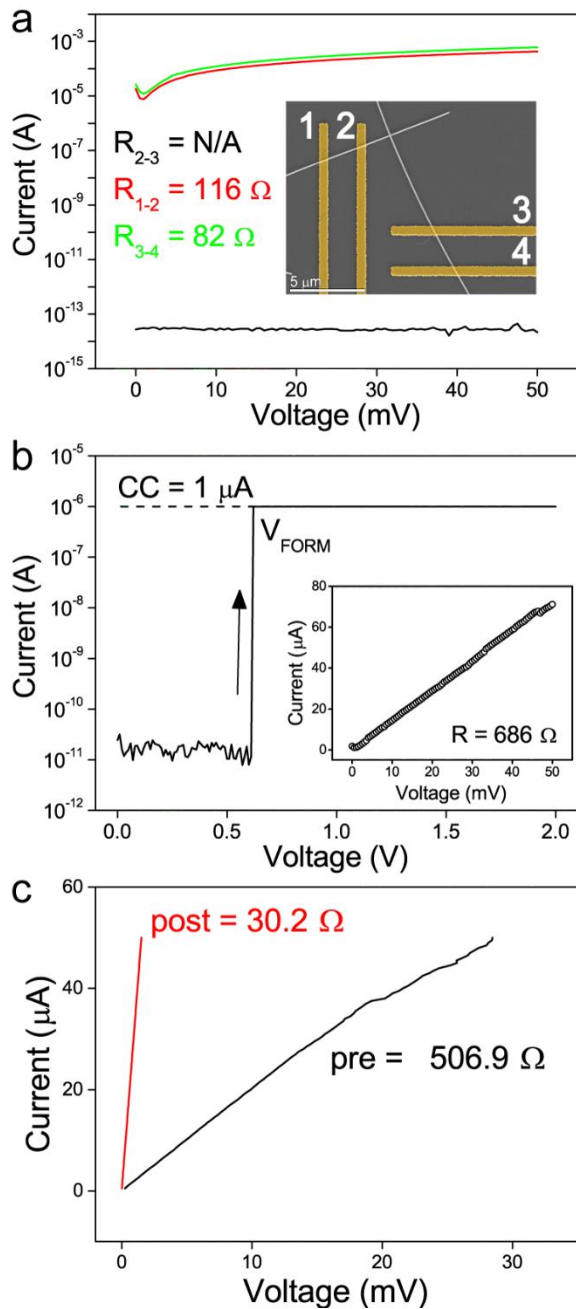


Figure 1. Electroforming a silver nanowire junction. (a) Initial low-bias voltage sweeps demonstrate the high resistance across the junction (electrodes 2-3) compared to the individual nanowire resistances (electrodes 1-2, and 3-4). Inset: false coloured SEM image of contacted junction highlighting the contacting electrodes. (b) Sweeping a bias across electrodes 2-3 allows the junction to be activated to a pre-defined compliance current of 1 μA, which in this case results in a measured resistance of 686 Ω (inset). Note

this activation step necessarily involves a 2-probe measurement as the junction resistance is higher than that of the inner circuit resistance. (c) Biasing the junction in the absence of a current limit results in a localised heating at the junction and a further reduction in resistance. The 4-probe resistance of the non-optimised junction in (b) is 506.9 Ω, demonstrating the contacts contribute over 180 Ω in the 2-probe measurement. The current-voltage plot in (c) shows that the 4-probe resistance drops to 30.2 Ω after a current of 5 mA has been passed through the junction, highlighting the effectiveness of the electroforming process.

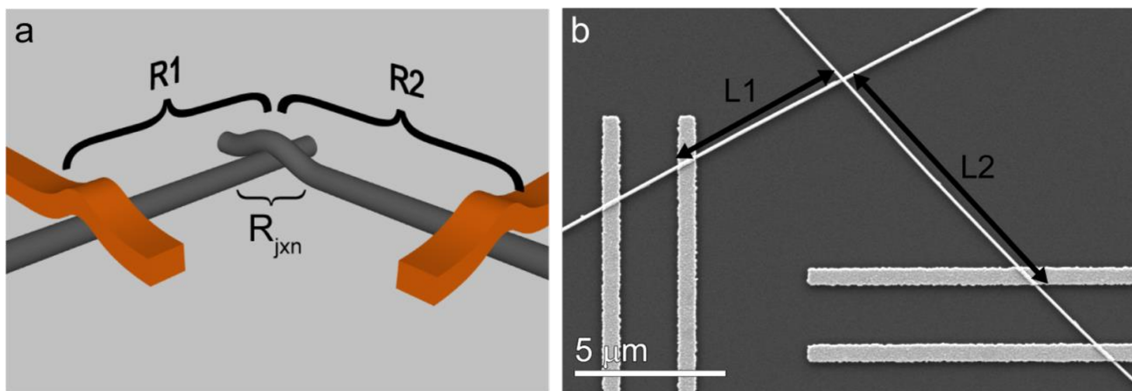
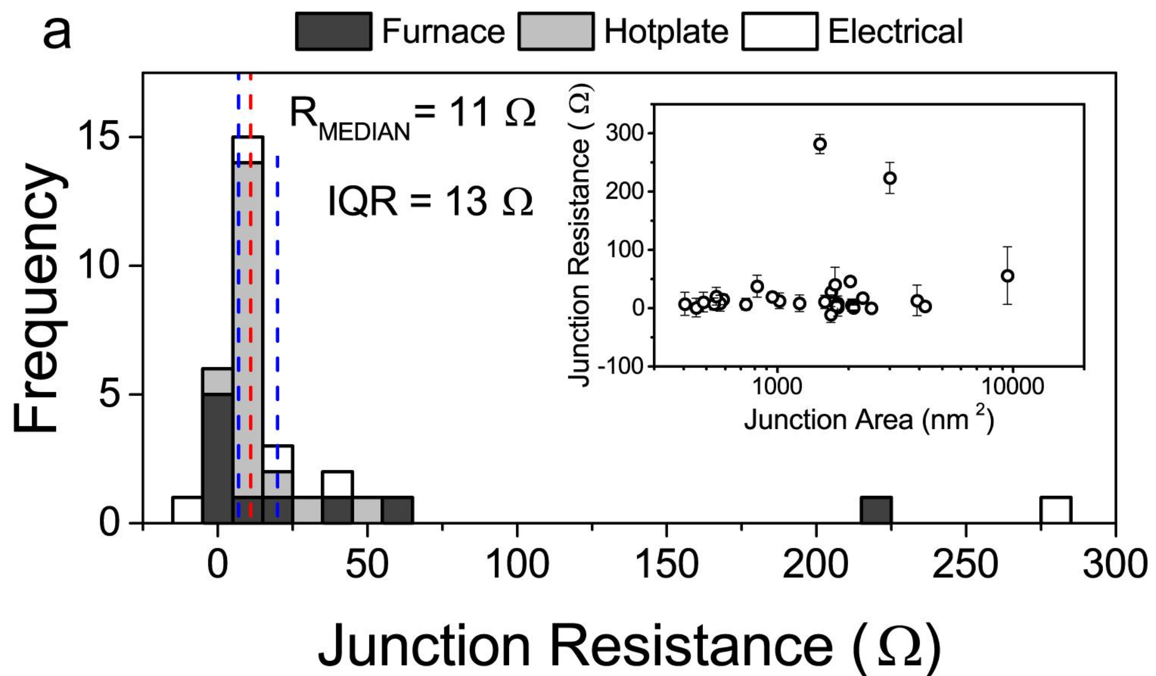


Figure 2. Extracting the junction resistance. (a) Measuring the nanowire diameter, length, and resistivity allows the resistance contribution of each nanowire, R1 and R2 respectively, to be calculated and removed from the measured resistance. (b) The length, L, is taken to be the distance from the outer edge of the inner contacting electrode to the centre of the junction, consistent with the work of Kolesnik *et al.*[34]



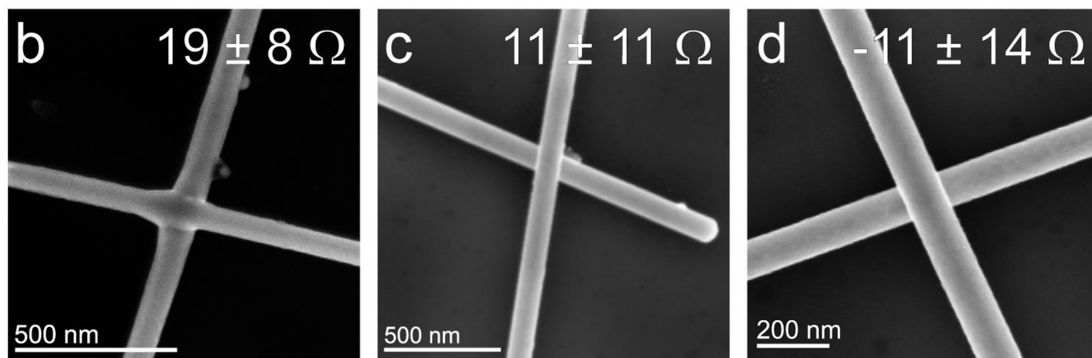


Figure 3. Resistance measurements on 32 Ag nanowire junctions. (a) Junction resistance data plotted as a function of frequency (bin size 10 Ω) for all three processing methods. A sharp peak is clear at a resistance value of 11 Ω. Also clear is that all processing methods produce similarly low junction resistances. The red dashed line indicates the median value of the distribution, while the blue dashed lines indicate the 1st and 3rd quartiles (interquartile range (IQR) = 13 Ω). Inset: R_{jxn} plotted as a function of calculated junction area (see text). Panels (b-d) show SEM images of nanowire junctions processed via furnace annealing (b), hotplate annealing (c), and electroforming (d) alongside the measured R_{jxn} value. Characteristic melting/welding of the junction is visible only in the

case of the furnace annealed wires, yet all three methods yield comparably low resistances.

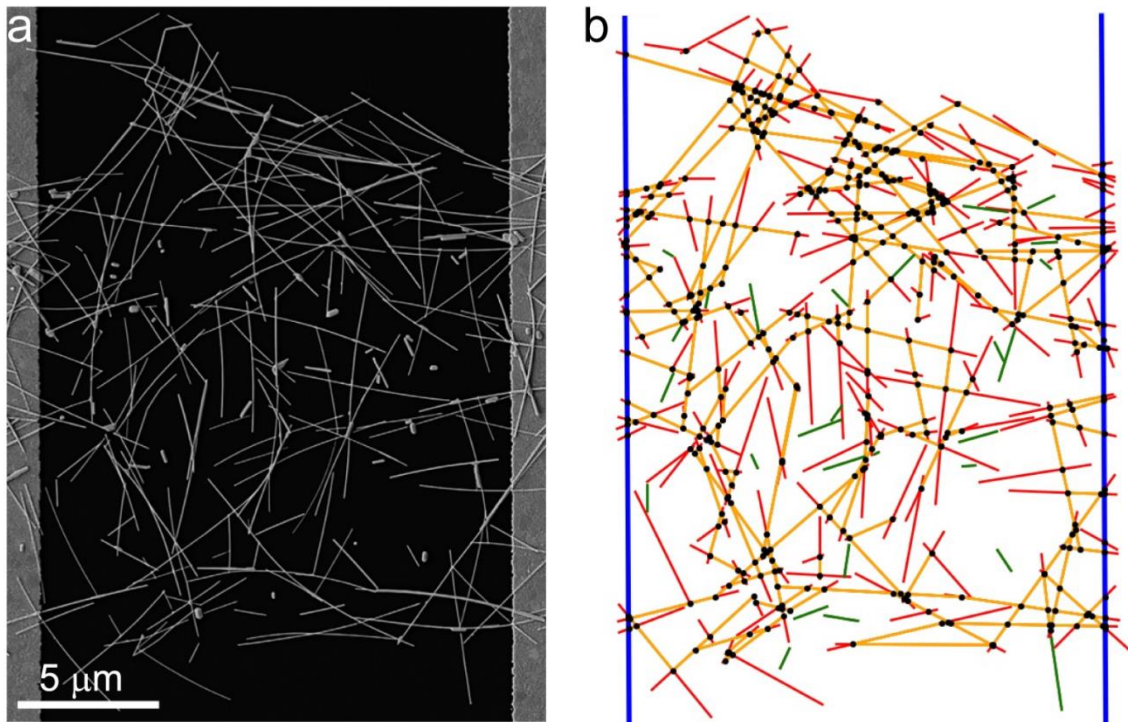


Figure 4 Mapping a real-world network. SEM image (a) and image of the same network represented as a 2D network of interconnected sticks (b). Each junction is indicated by a black dot, and each conductive path is highlighted in yellow, whilst dead paths are indicated in red. The experimental resistance of this network was measured to be 19 Ω, while the resistance calculated using the experimentally determined junction distribution was 26 ± 1 Ω, with 21 Ω of that coming from the nanowire skeleton itself.

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Author Contributions

A.T.B designed the experiments and wrote the paper, H.G.M. performed nanowire resistivity measurements and fabricated isolated networks for mapping, C.G.R. mapped networks and developed computational model, M.S.F. developed computational model, J.J.B. led overall effort and co-wrote the paper. H.G.M and C.G.R contributed equally to this work.

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ASSOCIATED CONTENT

Supporting Information Available: Further information on the nanowires used in this study may be found in the Supporting Information, including length/diameter statistics,

TEM image of a nanowire junction, as well as resistivity data and further SEM images of junctions under different processing conditions. Stick model images of all networks included in Table 2 are also included. This material is available free of charge *via* the Internet at http://pubs.acs.org.

REFERENCES

1. Na, S. I.; Kim, S. S.; Jo, J.; Kim, D. Y., Efficient and Flexible Ito-Free Organic Solar Cells Using Highly Conductive Polymer Anodes. *Adv. Mater.* **2008,** *20*, 4061-4067.

2. Kim, K. S.; Zhao, Y.; Jang, H.; Lee, S. Y.; Kim, J. M.; Kim, K. S.; Ahn, J. H.; Kim, P.; Choi, J. Y.; Hong, B. H., Large-Scale Pattern Growth of Graphene Films for Stretchable Transparent Electrodes. *Nature* **2009,** *457*, 706-710.

3. Zhu, Y.; Sun, Z.; Yan, Z.; Jin, Z.; Tour, J. M., Rational Design of Hybrid Graphene Films for High-Performance Transparent Electrodes. *ACS Nano* **2011,** *5*, 6472-6479.

4. De, S.; Higgins, T. M.; Lyons, P. E.; Doherty, E. M.; Nirmalraj, P. N.; Blau, W. J.; Boland, J. J.; Coleman, J. N., Silver Nanowire Networks as Flexible, Transparent, Conducting Films: Extremely High Dc to Optical Conductivity Ratios. *ACS Nano* **2009,** *3*, 1767-1774.

5. Hu, L. B.; Kim, H. S.; Lee, J. Y.; Peumans, P.; Cui, Y., Scalable Coating and Properties of Transparent, Flexible, Silver Nanowire Electrodes. *ACS Nano* **2010,** *4*, 2955-2963.

6. Wu, H.; Hu, L.; Rowell, M. W.; Kong, D.; Cha, J. J.; McDonough, J. R.; Zhu, J.; Yang, Y.; McGehee, M. D.; Cui, Y., Electrospun Metal Nanofiber Webs as High-Performance Transparent Electrode. *Nano Letters* **2010,** *10*, 4242-4248.

7. Rathmell, A. R.; Wiley, B. J., The Synthesis and Coating of Long, Thin Copper Nanowires to Make Flexible, Transparent Conducting Films on Plastic Substrates. *Adv. Mater.* **2011,** *23*, 4798-4803.

8. Lyons, P. E.; De, S.; Elias, J.; Schamel, M.; Philippe, L.; Bellew, A. T.; Boland, J. J.; Coleman, J. N., High-Performance Transparent Conductors from Networks of Gold Nanowires. *J. Phys. Chem. Lett.* **2011,** *2*, 3058-3062.

9. Langley, D.; Giusti, G.; Mayousse, C.; Celle, C.; Bellet, D.; Simonato, J. P., Flexible Transparent Conductive Materials Based on Silver Nanowire Networks: A Review. *Nanotechnology* **2013,** *24*, 452001.

10. Liang, J.; Li, L.; Tong, K.; Ren, Z.; Hu, W.; Niu, X.; Chen, Y.; Pei, Q., Silver Nanowire Percolation Network Soldered with Graphene Oxide at Room Temperature and Its Application for Fully Stretchable Polymer Light-Emitting Diodes. *ACS Nano* **2014**.

11. Jurewicz, I.; Fahimi, A.; Lyons, P. E.; Smith, R. J.; Cann, M.; Large, M. L.; Tian, M.; Coleman, J. N.; Dalton, A. B., Insulator-Conductor Type Transitions in Graphene-Modified Silver Nanowire Networks: A Route to Inexpensive Transparent Conductors. *Adv. Funct. Mater.* **2014**.

12. An, B. W.; Hyun, B. G.; Kim, S.-Y.; Kim, M.; Lee, M.-S.; Lee, K.; Koo, J. B.; Chu, H. Y.; Bae, B.-S.; Park, J.-U., Stretchable and Transparent Electrodes Using Hybrid Structures of Graphene–Metal Nanotrough Networks with High Performances and Ultimate Uniformity. *Nano Letters* **2014,** *14*, 6322-6328.

13. Shi, L.; Wang, R.; Zhai, H.; Liu, Y.; Gao, L.; Sun, J., A Long-Term Oxidation Barrier for Copper Nanowires: Graphene Says Yes. *Phys. Chem. Chem. Phys.* **2015**.

14. Zhu, S.; Gao, Y.; Hu, B.; Li, J.; Su, J.; Fan, Z.; Zhou, J., Transferable Self-Welding Silver Nanowire Network as High Performance Transparent Flexible Electrode. *Nanotechnology* **2013,** *24*, 335202.

15. De, S.; Coleman, J. N., Are There Fundamental Limitations on the Sheet Resistance and Transmittance of Thin Graphene Films? *ACS Nano* **2010,** *4*, 2713-2720.

16. Geng, H.-Z.; Kim, K. K.; So, K. P.; Lee, Y. S.; Chang, Y.; Lee, Y. H., Effect of Acid Treatment on Carbon Nanotube-Based Flexible Transparent Conducting Films. *J. Am. Chem. Soc.* **2007,** *129*, 7758-7759.

17. Wang, J.; Jiu, J.; Araki, T.; Nogi, M.; Sugahara, T.; Nagao, S.; Koga, H.; He, P.; Suganuma, K., Silver Nanowire Electrodes: Conductivity Improvement without Post-Treatment and Application in Capacitive Pressure Sensors. *Nano-Micro Lett.* **2014**, 1-8.

18. Sorel, S.; Lyons, P. E.; De, S.; Dickerson, J. C.; Coleman, J. N., The Dependence of the Optoelectrical Properties of Silver Nanowire Networks on Nanowire Length and Diameter. *Nanotechnology* **2012,** *23*, 185201.

19. Bergin, S. M.; Chen, Y. H.; Rathmell, A. R.; Charbonneau, P.; Li, Z. Y.; Wiley, B. J., The Effect of Nanowire Length and Diameter on the Properties of Transparent, Conducting Nanowire Films. *Nanoscale* **2012,** *4*, 1996-2004.

20. Scardaci, V.; Coull, R.; Lyons, P. E.; Rickard, D.; Coleman, J. N., Spray Deposition of Highly Transparent, Low-Resistance Networks of Silver Nanowires over Large Areas. *Small* **2011,** *7*, 2621-2628.

21. Lee, J.-Y.; Connor, S. T.; Cui, Y.; Peumans, P., Solution-Processed Metal Nanowire Mesh Transparent Electrodes. *Nano Letters* **2008,** *8*, 689-692.

22. Leem, D.-S.; Edwards, A.; Faist, M.; Nelson, J.; Bradley, D. D. C.; de Mello, J. C., Efficient Organic Solar Cells with Solution-Processed Silver Nanowire Electrodes. *Adv. Mater.* **2011,** *23*, 4371-4375.

23. Liu, C.-H.; Yu, X., Silver Nanowire-Based Transparent, Flexible, and Conductive Thin Film. *Nanoscale Res. Lett.* **2011,** *6*, 75.

24. Langley, D.; Lagrange, M.; Giusti, G.; Jimenez, C.; Bréchet, Y.; Nguyen, N. D.; Bellet, D., Metallic Nanowire Networks: Effects of Thermal Annealing on Electrical Resistance. *Nanoscale* **2014,** *6*, 13535-13543.

25. Sachse, C.; Müller-Meskamp, L.; Bormann, L.; Kim, Y. H.; Lehnert, F.; Philipp, A.; Beyer, B.; Leo, K., Transparent, Dip-Coated Silver Nanowire Electrodes for Small Molecule Organic Solar Cells. *Org. Electron.* **2013,** *14*, 143-148.

26. Tokuno, T.; Nogi, M.; Karakawa, M.; Jiu, J.; Nge, T. T.; Aso, Y.; Suganuma, K., Fabrication of Silver Nanowire Transparent Electrodes at Room Temperature. *Nano Res.* **2011,** *4*, 1215-1222.

27. Garnett, E. C.; Cai, W.; Cha, J. J.; Mahmood, F.; Connor, S. T.; Greyson Christoforo, M.; Cui, Y.; McGehee, M. D.; Brongersma, M. L., Self-Limited Plasmonic Welding of Silver Nanowireâ junctions. *Nat. Mater.* **2012,** *11*, 241-249.

28. Han, S.; Hong, S.; Ham, J.; Yeo, J.; Lee, J.; Kang, B.; Lee, P.; Kwon, J.; Lee, S. S.; Yang, M. Y., Fast Plasmonic Laser Nanowelding for a Cu-Nanowire Percolation Network for Flexible Transparent Conductors and Stretchable Electronics. *Adv. Mater.* **2014,** *26*, 5808-5814.

29. Nirmalraj, P. N.; Bellew, A. T.; Bell, A. P.; Fairfield, J. A.; McCarthy, E. K.; O'Kelly, C.; Pereira, L. F. C.; Sorel, S.; Morosan, D.; Coleman, J. N.*, et al.*, Manipulating Connectivity and Electrical Conductivity in Metallic Nanowire Networks. *Nano Letters* **2012,** *12*, 5966-5971.

30. Bellew, A. T.; Bell, A. P.; McCarthy, E. K.; Fairfield, J. A.; Boland, J. J., Programmability of Nanowire Networks. *Nanoscale* **2014,** *6*, 9632-9639.

31. Mutiso, R. M.; Sherrott, M. C.; Rathmell, A. R.; Wiley, B. J.; Winey, K. I., Integrating Simulations and Experiments to Predict Sheet Resistance and Optical Transmittance in Nanowire Films for Transparent Conductors. *ACS Nano* **2013,** *7*, 7654-7663.

32. Song, T.-B.; Chen, Y.; Chung, C.-H.; Yang, Y.; Bob, B.; Duan, H.-S.; Li, G.; Tu, K.-N.; Huang, Y.; Yang, Y., Nanoscale Joule Heating and Electromigration Enhanced Ripening of Silver Nanowire Contacts. *ACS Nano* **2014,** *8*, 2804-2811.

33. Jagota, M.; Tansu, N., Conductivity of Nanowire Arrays under Random and Ordered Orientation Configurations. *Sci. Rep.* **2015,** *5*.

34. Waser, R.; Dittmann, R.; Staikov, G.; Szot, K., Redox-Based Resistive Switching Memories, Nanoionic Mechanisms, Prospects, and Challenges. *Adv. Mater.* **2009,** *21*, 2632-2663.

35. M., K. M.; Hansel, S.; Lutz, T.; Kinahan, N.; Boese, M.; Krstic, V., Resolving in Situ Specific-Contact, Current-Crowding, and Channel Resistivity in Nanowire Devices: A Case Study with Silver Nanowires. *Small* **2011,** *7*, 2873-2877.

36. Huang, Q.; Lilley, C. M.; Bode, M., Surface Scattering Effect on the Electrical Resistivity of Single Crystalline Silver Nanowires Self-Assembled on Vicinal Si (001). *Appl. Phys. Lett.* **2009,** *95*, 103112.

37. da Rocha, C. G.; Manning, H. G.; O'Callaghan, C.; Ritter, C.; Bellew, A. T.; Boland, J. J.; Ferreira, M. S., Ultimate Conductivity Performance in Metallic Nanowire Networks. *Nanoscale* **2015,** *7*, 13011-13016.

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